Classification, Terminology, and Application of the Modular Multilevel Cascade Converter (MMCC)

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***Abstract*—This paper discusses the modular multilevel cascade converter (MMCC) family based on cascade connection of multiple bidirectional chopper cells or single-phase full-bridge cells. The MMCC family is classified from circuit configuration as follows: the single-star bridge cells (SSBC); the single-delta bridge cells (SDBC); the double-star chopper cells (DSCC); and the double-star bridge cells (DSBC). The term MMCC corresponds to a family name in a person while, for example, the term SSBC corresponds to a given name. Therefore, the term "MMCC–SSBC" can identify the circuit configuration without any confusion. Among the four MMCC family members, the SSBC and DSCC are more practical in cost, performance, and market than the others although a distinct difference exists in application between the SSBC and DSCC. This paper presents application examples of the SSBC to a battery energy storage system (BESS), the SDBC to a static synchronous compensator (STATCOM) for negative-sequence reactive-power control, and the DSCC to a motor drive for fans and blowers, along with their experimental results.**

***Index Terms*—Battery energy storage, modular structure, motor drives, multilevel converters.**

I. Introduction

SINCE the middle of the 1990s, Robicon Corporation, presently a part of Siemens, has put a medium-voltage high-power motor drive with a multilevel pulsewidth modulation (PWM) inverter into practical use [1]. The emergence of this motor drive surprised and impressed research scientists and engineers who were engaged in research and development of medium-voltage motor drives. The per-phase circuit configuration of the multilevel inverter is based on cascade connection of the ac output terminals of modular single-phase full-bridge or "H-bridge" inverter cells. However, it requires a complicated multiwinding phase-shifted line-frequency transformer for delivering electric power to all the floating H-bridge inverter cells. Before such a medium-voltage high-power motor drive was brought to the market, a few pioneering papers on the "modular multilevel structure" had been presented and published, taking the form of a single-phase circuit for plasma stabilization [2] and a three-phase circuit for motor drives [3].

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In the middle of the 1990s, Lai and Peng presented a static synchronous compensator (STATCOM) for reactive-power control, which is based on cascade connection of modular H-bridge converter cells with stair-case modulation (SCM) [4], [5]. It was followed by a battery energy storage system (BESS) with SCM for motor drives [6]. These are characterized by eliminating the complicated multiwinding phase-shifted line-frequency transformer from the power conversion systems.

Marquardt and coauthors presented another power conversion circuit referred to as a "modular multilevel converter" and its basic operating principle [7], [8]. Although the circuit configuration of each arm was described in [9], research has been conducted on the viability and effectiveness of the modular multilevel converter intended for applications to HVDC and back-to-back (BTB) systems [10], [11]. However, the sound of the modular multilevel converter makes it impossible for the beginners of power electronics to distinguish the circuit configuration from the others because the terms "modular" and "multilevel" do not have enough information to identify the circuit configuration. Moreover, it is reasonable to call the modular multilevel converter as a "cascade multilevel converter" because the converter is based on cascade connection of the lower dc voltage terminals of modular bidirectional choppers. Of course, it is allowable to use the term "modular multilevel converter" as a proper noun.

On the other hand, the multilevel inverter developed and commercialized by Robicon Corporation is referred to as a "cascade multilevel inverter," a "series-connected H-bridge multilevel inverter," or a "chain-link multilevel inverter" at present. That is, different manufactures use different names, like trade names. However, the multilevel inverter can be considered as a "modular multilevel inverter" because it is one of the modular multilevel inverters based on modular H-bridge cells. This may lead to the following confusion: when a power electronics engineer uses either "modular multilevel converter" or "cascade multilevel converter" in his/her technical paper/article or presentation, the other engineers cannot identify the circuit configuration or may have a misunderstanding about it in the worst case.

This paper classifies the modular multilevel cascade converter (MMCC) family, the name of which merges both terms "cascade multilevel converter" and "modular multilevel converter" together [12]. The author gives appropriate names to the four family members with focus on circuit configuration, thus resulting in identifying the individual circuit configurations. Then, this paper makes a detailed description of comparisons among the four members in terms of circuit configuration, circulating current, and application. Finally, this paper has an intensive discussion on applications of three promising family members, the

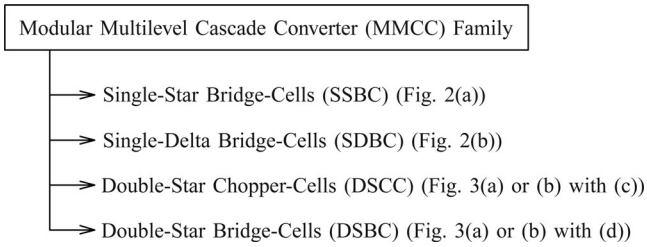

Fig. 1. Classification and terminology of the MMCC family.

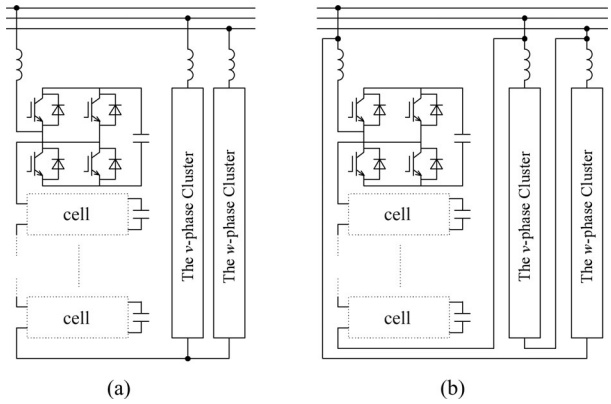

Fig. 2. Possible circuit configurations of the SSBC and the SDBC without common dc link. (a) SSBC. (b) SDBC.

SSBC, SDBC, and DSCC to a grid-level BESS, a STATCOM for negative-sequence reactive-power control, and an adjustable-speed motor drive, respectively. Experimental results obtained from the three downscaled systems designed and constructed in the author's laboratory are shown to justify the identity of each MMCC family member.

II. Classification and Terminology

Fig. 1 shows the classification and terminology of the MMCC family in a broad sense. Figs. 2 and 3 depict the four circuit configurations belonging to the family. The common concepts hidden in the family members are both "modular" structure and "cascade" connection. These concepts allow power electronics engineers to use the term "modular multilevel cascade converter (MMCC)" as a family name. However, only the family name cannot identify the individual family members. Therefore, a given name should be introduced to each family member as if to identify each circuit configuration.

Fig. 2(a) and (b) shows the following two circuit configurations, respectively: the single-star bridge cells (SSBC) and the single-delta bridge cells (SDBC). The reason for naming is that both are based on three strings of multiple H-bridge cells with either star or delta connection. This paper refers to a string of multiple H-bridge cells as a "cluster" to distinguish it from the existing terms "arm" and "leg."

Fig. 3 shows the other two circuit configurations: the double-star chopper-cells (DSCC) for the combination of (a) or (b) with (c); and the double-star bridge-cells (DSBC) for the combination of (a) or (b) with (d), respectively. The reason for naming is that the DSCC is based on two sets of star-configured converters in

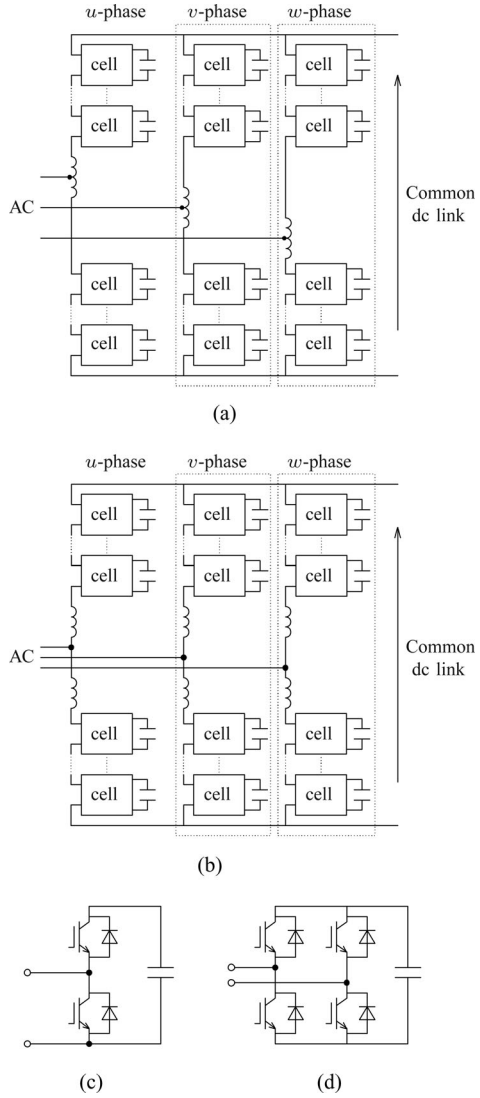

Fig. 3. Possible circuit configurations of the DSCC and the DSBC with a common dc link. (a) Power circuit using coupled buffer inductors. (b) Power circuit using noncoupled buffer inductors. (c) Chopper cell (DSCC). (d) Bridge cell (DSBC).

which the low-voltage sides of multiple bidirectional chopper cells are cascaded to constitute each arm. The DSBC is based on two sets of star-configured converters in which the ac sides of multiple H-bridge cells are cascaded to constitute each arm. The slight difference in circuit configuration between Fig. 3(a) and (b) comes from the buffer inductor(s) sitting between the positive and negative arms in each leg. Note that the buffer inductor(s) would play an important role, not only in supporting a voltage difference between the total of multiple chopper or bridge cells in each leg and the common dc link, but also in controlling the circulating current in each leg. Fig. 3(a) uses a single coupled or center-tapped inductor per leg while Fig. 3(b) uses two noncoupled inductors. The single coupled inductor is smaller in size and lighter in weight than the total of the two noncoupled inductors. Therefore, in particular, applications of the DSCC to motor drives would prefer (a) to (b) because the ac terminals of (a) can be connected directly to the motor terminals.

TABLE I
COMPARISONS AMONG THE FOUR MMCC FAMILY MEMBERS

Terminology	SSBC (Fig. 2(a))	SDBC (Fig. 2(b))	DSCC (Fig. 3(a) or (b) with (c))	DSBC (Fig. 3(a) or (b) with (d))
Main objectives	Positive-sequence reactive power and/or active power	Negative-sequence reactive power and/or active power	Rectification and inversion Negative-sequence reactive power	Rectification and inversion Ac-ac direct conversion
Cell-count ratio	1	$\sqrt{3}$	4	2–4 (depend on circuit design)
Circulating current	No	One degree of freedom	Two or three degrees of freedom	Two or three degrees of freedom
Buffer inductor	No	No	One inductor per leg in Fig. 3(a) Two inductors per leg in Fig. 3(b)	One inductor per leg in Fig. 3(a) Two inductors per leg in Fig. 3(b)
Grid inductor	Yes	Yes	Yes in Fig. 3(a) No in Fig. 3(b)	Yes in Fig. 3(a) No in Fig. 3(b)
Motor drives	No, but limited exceptions exist.	No, but limited exceptions exist.	Fans and blowers	Fans and blowers
Grid applications	STATCOM (voltage regulation) Battery energy storage system	STATCOM (flicker compensation) Battery energy storage system	HVDC/BTB system STATCOM (flicker compensation)	Wind/solar power conditioning New matrix converter
Practicability	+++++	+++	++++	++

Thus, the MMCC–SSBC, MMCC–SDBC, MMCC–DSCC, and MMCC–DSBC should be used as the full names of the four members. From a practical point of view, however, the family name "MMCC" can be eliminated from the four full names as long as no confusion occurs in circuit configuration.

III. COMPARISONS OF THE MMCC FAMILY

Table I summarizes comparisons among the four MMCC members from various points of view. Generally, the SSBC and SDBC are similar in application, while the DSCC and DSBC are similar in circuit configuration. This suggests that a group of the SSBC and SDBC has a significant difference in performance and application from that of the DSCC and DSBC. The difference results mainly from two additional dc or ac terminals existing in Fig. 3(a) and (b). The "cell-count ratio" in the third row of Table I means the ratio of the cell count of each MMCC member with respect to that of the SSBC under the following assumptions: the insulated-gate bipolar transistors (IGBTs) used in the four MMCC members have the same blocking voltage, and the four MMCC members have the same power and voltage ratings. As a result, the IGBTs have different current ratings because the count of the IGBTs is different each other. The "practicability" in the last row of Table I includes technical aspects as well as the market size of each member.

Paying attention to similarity and difference among the four members results in making the following descriptions.

A. Three-Terminal and Five-Terminal Circuits

Both SSBC and SDBC are the so-called three-terminal circuits if the neutral point of star connection is neglected from the SSBC. This makes it impossible to apply both converters to motor drives as long as a single common dc source is available. However, both converters are applicable to motor drives when available are galvanically isolated multiple dc voltage sources based on battery modules or stacks [6], the combination of a multiwinding line-frequency transformer with three-phase diode rectifiers [1], or bidirectional isolated dc–dc converters [13].

On the other hand, both DSCC and DSBC are "five-terminal circuits" because both are allowed to use the two neutral points of star-configured circuits as the two dc terminals. These terminals can be connected to the dc output terminals of a three-phase diode rectifier. This makes it possible to use both DSCC and DSBC as multilevel inverters for motor drives.

B. No Circulating Current in the SSBC

The SSBC has the capability of controlling positive-sequence leading and lagging reactive power. Unlike the SDBC, however, the SSBC has no capability of releasing negative-sequence reactive power to the grid or absorbing it from the grid, because no circulating current flows inside the SSBC. Therefore, applications of the SSBC are limited to a STATCOM for positive-sequence reactive-power control, and a BESS devoting itself mainly to active-power control at the lowest cost among the four members. The reason is that the SSBC has a minimum cell count among the four MMCC family members, as shown in Table I.

The SSBC can add a common zero-sequence voltage to each of the three cluster voltages. This zero-sequence voltage can be used for achieving voltage balancing control of all the floating split dc capacitors in the STATCOM [14], and for achieving state-of-charge (SOC) balancing control, fault-tolerant control, and active-power control of individual converter cells in the BESS [15]–[17]. Note that no change occurs in the three-phase line-to-line voltages at the ac side of the three clusters even if the zero-sequence voltage is applied. As a result, no change occurs in the three-phase supply currents.

C. Circulating Current in the SDBC, DSCC, and DSBC

The others, the SDBC, DSCC, and DSBC have the capability of controlling negative-sequence reactive power because they allow a current to circulate among three clusters for the SDBC and a current to circulate through the positive and negative arms in each leg for both DSCC and DSBC. The circulating current plays an essential role in exchanging active power among the three clusters and legs although the circulating current is accompanied by a slight increase in conducting and switching losses. The SDBC has one degree of freedom in the circulating current. The DSCC and DSBC have two degrees of freedom when nothing is installed on their dc terminals, or three degrees of freedom when either a dc voltage source or a dc-link capacitor is connected.

When the SDBC is used as a STATCOM, the amplitude of the circulating line-frequency current is proportional to the amount of negative-sequence reactive power, whereas it is independent

of the amount of positive-sequence reactive power. When the DSCC is used as an inverter for a motor drive, the amplitude of the circulating dc current is proportional to the amount of active power at the motor terminals, whereas it is independent of the amount of reactive power.

Like the SDBC, DSCC can be used as a STATCOM for negative-sequence reactive-power control. However, the cell-count ratio of the DSCC with respect to the SDBC can be calculated as $4/\sqrt{3} = 2.3$ from the third row of Table I. This means that the DSCC would be inferior to the SDBC in terms of cost when the two MMCC members are applied to the STATCOM for negative-sequence reactive-power control.

D. Differences Between the DSCC and the DSBC

The circuit configurations of the DSCC and DSBC look similar, and their control systems are almost the same. However, their applications are different from a practical point of view.

The DSCC is applicable to medium-voltage motor drives for fans, blowers, and compressors. It is also applicable to HVDC transmission systems, and a BTB systems for achieving frequency change between two power systems with different line frequencies, and/or asynchronous link between two power systems with the same line frequency.

The DSBC is superior to the DSCC in terms of tolerating a broad range of variations in the dc-link voltage, because the DSBC has additional buck and boost functions of the dc-link voltage for rectification and inversion. Therefore, the DSBC is suitable to a power conditioning system (PCS) for renewable resources such as wind power and solar power, in which the dc-link input voltage varies with wind and weather conditions. Moreover, the DSBC can act as a three-to-single-phase direct frequency changer that is similar to a traditional line-commutated cycloconverter using thyristors. However, the DSBC is different from the cycloconverter in terms of unity-power-factor operation at the input side, and three-phase sinusoidal current waveforms at both input and output sides.

IV. Application of the SSBC to a BESS

It is promising to apply the SSBC to a grid-level BESS that will take a part of the so-called load-frequency control to balance electric-power supply and demand over a period of shorter than 30 min in power systems. What is the most interesting to such a grid-level storage system is to allow the SSBC to use cost-effective battery stacks with a nominal dc voltage as low as 700 V. As a result, it would be possible to design, construct, and install the grid-level BESS rated at 10 MW of power and 10 MW·h of energy.

A. Circuit Configuration

Fig. 4 shows the system configuration of an experimental SSBC-based BESS rated at 200 V, 10 kW, and 3.6 kW·h [15]–[17]. Circuit breakers CB1 and CB2, magnetic contactors MC1 and MC2, and resistors R_1 and R_2 are used for protection against overcurrent and inrush current during faults and start-up. Table II summarizes the circuit parameters. The experimental system has a cascade number or per-cluster cell count $N = 3$. Each of the nine converter cells is equipped with a nickel–metal–hydride (NiMH) battery module at its dc side. Each battery module is rated at 72 V and 5.5 A·h, consisting of series connection of 60 battery cells, where the dc voltage ranges from 66 to 84 V. The total rated energy capacity is 13 MJ or 3.6 kW·h $(=72\,\mathrm{V} \times 5.5\,\mathrm{A} \times 9)$. Elimination of the battery module from the dc side of each H-bridge converter cell allows the experimental system to act as the SSBC-based STATCOM described in [14].

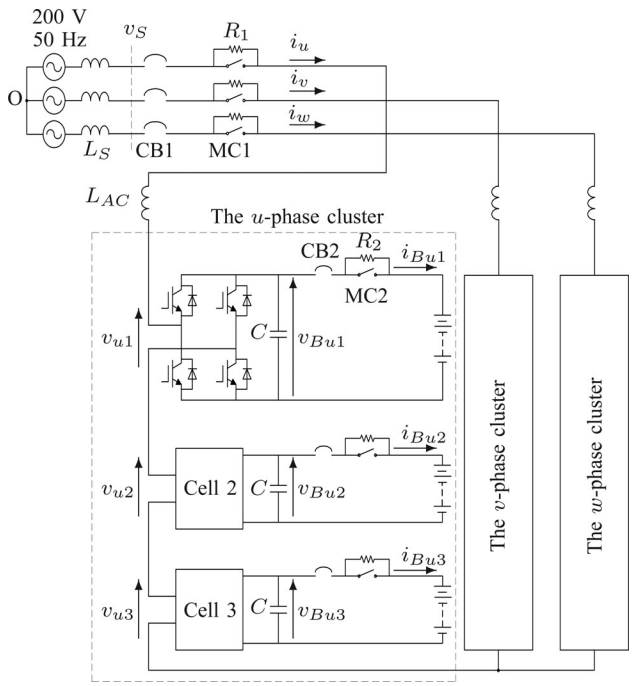

Fig. 4. Experimental system configuration of the 200-V, 10-kW, 3.6-kW·h downscaled energy storage system based on the SSBC.

TABLE II
Circuit Parameters of the SSBC-Based BESS

Nominal line-to-line rms voltage	V_S	200 V
Power rating	P	10 kW
Cascade number	N	3
AC inductor	L_{AC}	1.2 mH (10%)
Background system inductance	L_S	48 μH (0.4%)
Starting Resistors	$R_1,\ R_2$	10 Ω, 20 Ω
Nominal battery-module voltage	V_B	72 V
DC capacitor	C	16.4 mF
Unit capacitance constant [19]	H	38 ms at 72 V
NiMH battery module		72 V and 5.5 Ah
PWM carrier frequency		800 Hz
Equivalent carrier frequency		4.8 kHz

Values in ( ) are on a three-phase, 200-V, 10-kW, 50-Hz base.

B. Control System

Fig. 5 shows the control system based on a fully digital controller using a digital signal processor (DSP) and multiple field-programmable gate arrays (FPGAs). Each battery module is equipped with the battery management system (BMS) that provides the functions of monitoring and controlling

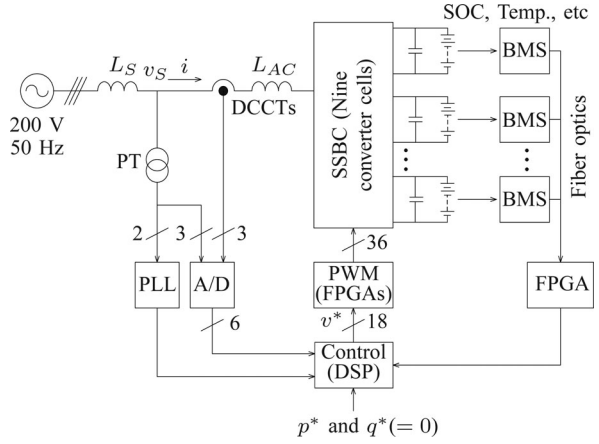

Fig. 5. Control system for the SSBC-based BESS.

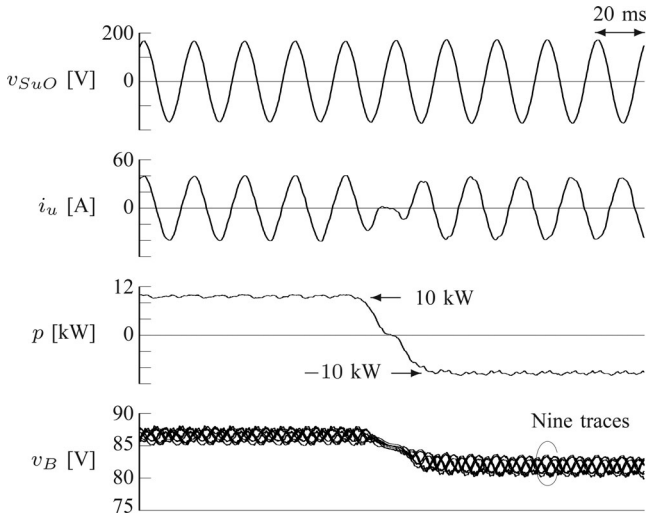

Fig. 6. Experimental waveforms obtained from the SSBC-based BESS when p^* was changed from 10 to -10 kW in 30 ms with a mean SOC value of 70%.

the respective battery module to protect it against abnormal conditions. The nine H-bridge converter cells are controlled by phase-shifted unipolar sinusoidal PWM with a carrier frequency of 800 Hz. The resulting line-to-neutral voltage is a seven-level waveform with an equivalent carrier frequency of 4.8 kHz ($=2 \times 3$ cells $\times$ 800 Hz). The instantaneous real and imaginary power references are denoted as p^* and q^* [20], [21]. Note that a condition of $q^* = 0$ is applied to the following experiments. In [15]–[17], a detailed description of the control method including the phase-shift PWM is given.

C. Experimental Waveforms

Fig. 6 shows experimental waveforms from charging to discharging operation with a ramp change in active power from $+10$ to -10 kW in 30 ms with a mean SOC value around 70%.[1] The waveforms of v_{SuO} and i_u were in phase during charging, while they were out of phase by 180° during discharging, because this system was operated with a condition of $q^* = 0$. Note

[1]The experimental waveforms in Figs. 6, 8, 10, 11, and 14 were taken in a PC through the YOKOGAWA WE7000 PC-based data acquisition system with different sampling rates, according to their time scales.

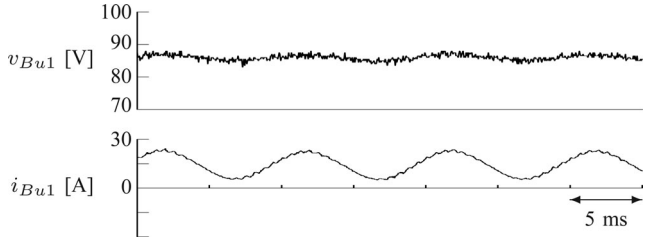

Fig. 7. Experimental battery-module voltage and current waveforms obtained from the SSBC-based BESS during charging at 10 kW with a mean SOC value of 65%.

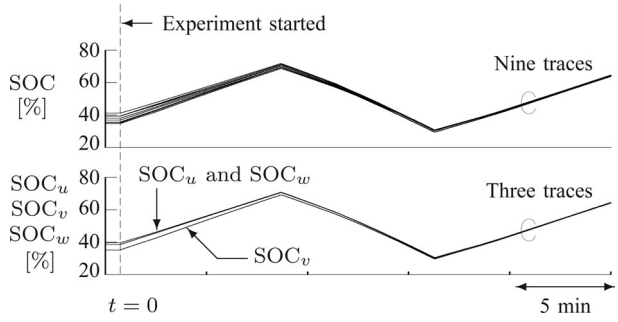

Fig. 8. Experimental waveforms obtained from the SSBC-based BESS to verify the effectiveness of the SOC-balancing control, where a mean SOC value was kept between 30% and 70% with $p^* = 10$ kW and $q^* = 0$.

that the battery-module dc voltages changed from 87 to 82 V as soon as the power reference p^* was changed from $+10$ to -10 kW. This voltage difference resulted from a voltage across an equivalent series resistance existing in the individual battery modules.

Fig. 7 shows the voltage and current waveforms of a battery module in the u-cluster during charging at 10 kW with a mean SOC value of 65%. The waveform of v_{Bu1} contained a 100-Hz component of 2 V (peak-to-peak), and the waveform of i_{Bu1} contained a 100-Hz component of 17.5 A (peak-to-peak). They are in phase so that the equivalent series impedance of the battery module can be considered purely resistive. The equivalent series resistance is estimated to be 115 mΩ ($=2\,\mathrm{V}/17.5\,\mathrm{A}$). The resistance of a standalone battery module was measured to be 133 mΩ at a SOC value of 65% and a battery temperature of 30 °C. These two equivalent series resistances are almost equal.

Fig. 8 shows the nine SOC values of the battery modules in the upper part and the three mean SOC values of the u-, v- and w-clusters in the lower part. Before starting the experiment ($t = 0$), the SOC values of the nine battery modules had a maximal imbalance of 5% between the lowest and highest ones. However, when the SOC-balancing control was enabled along with $p^* = \pm 10$ kW at $t = 0$, the nine SOC values gradually started to converge together. In about 15 min, all the SOC values became equal. This experiment justified the effectiveness of the SOC-balancing control [15]. Since the SOC-balancing control would be always active in an actual system, no SOC imbalance would occur among the battery modules except for a short-tem period of start-up.

The SOC-balancing control is indispensable for putting the SSBC-based BESS into practical use. In addition, fault-tolerant

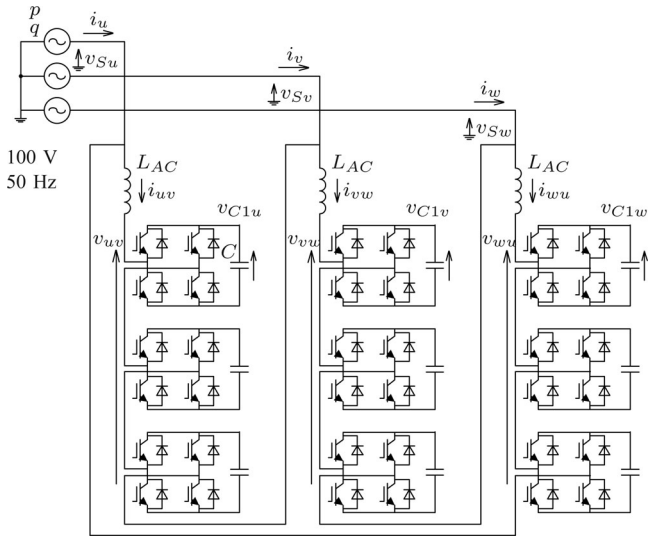

Fig. 9. Experimental system configuration of the 100-V 5-kV·A STATCOM based on the SDBC.

control and active-power control of individual converter cells and/or battery modules are crucial for enhancing reliability and overcoming a fault of a convert cell and/or battery module, which have been described in [16] and [17].

V. Application of the SDBC to a STATCOM for Negative-Sequence Reactive-Power Control

An arc furnace draws randomly changing active power as well as fluctuating positive- and negative-sequence reactive powers, according to the melting conditions of collective iron slabs. In particular, a large-capacity arc furnace may cause the so-called voltage flicker or low-frequency voltage fluctuation to other consumers receiving electric power from the same feeder. When the SDBC is used as a STATCOM, it can control not only positive-sequence reactive power but also negative-sequence reactive power, so as to compensate for both reactive powers drawn by the arc furnace. A few papers have made a brief description of a SDBC-based STATCOM [4], [5], [18]. However, no paper has been presented or published on experimental confirmation of operating performance of the SDBC-based STATCOM intended for negative-sequence reactive-power control.

A. Circuit Configuration

Fig. 9 shows the circuit configuration of the SDBC-based STATCOM used for the following experiment. Table III summarizes the circuit parameters. A string of three cascade H-bridge cells per phase is referred to as a "cluster." Each of the three clusters is equipped with an ac inductor $L_{\rm ac}$. Thus, the delta connection of three sets of clusters and ac inductors forms the DSBC.

The following equations on currents come into existence in Fig. 9.

$$i_u = i_{uv} - i_{wu} \tag{1}$$

$$i_v = i_{vw} - i_{uv} \tag{2}$$

$$i_w = i_{wu} - i_{vw}. \tag{3}$$

TABLE III
Circuit Parameters of the SDBC-Based STATCOM

Nominal line-to-line rms voltage	V_S	100 V
Power rating	P	5 kVA
Line frequency	ω/π	50 Hz
Cascade number	N	3
Rated line current	I	29 A
Rated cluster current	$I/\sqrt{3}$	17 A
AC inductor	L_{AC}	1.2 mH (6%)
DC capacitor	C	16.4 mF
DC capacitor voltage reference	V_C^*	60 V
Unit capacitance constant [19]	H	53 ms
PWM carrier frequency		2 kHz
Equivalent carrier frequency		12 kHz

Value in ( ) is on a three-phase, 100-V, 5-kVA, 50-Hz base.

Here, i_u, i_v, and i_w represent three-phase line currents while i_{uv}, i_{vw}, and i_{wu} three-phase cluster currents. The circulating current, that is the current circulating through the delta-configured clusters, is denoted as i_Z. Thus, it is defined by

$$i_Z = \frac{1}{3}(i_{uv} + i_{vw} + i_{wu}). \tag{4}$$

B. Control Method

The SSBC and SDBC look similar in circuit topology, as shown in Fig. 2(a) and (b). However, the following significant difference exists in circuit operation between the two: the SSBC has no circulating current, whereas the SDBC can control it. The control method of the SDBC-based STATCOM can be divided into instantaneous real and imaginary power control and voltage-balancing control. The former has been confirmed firmly, and has been applied to PCS for grid connection [21]. The latter is indispensable to the STATCOM in terms of achieving voltage balancing of all the nine floating split dc capacitors. It consists of overall voltage control, clustered balancing control, and individual balancing control, each of which constitutes a voltage major loop. The clustered balancing control is characterized by including the circulating-current control constituting a current minor loop in it. Note that the voltage-balancing control is not to regulate the "instantaneous" voltages of the dc capacitors at their voltage reference, but to regulate the "mean" voltages over a time of half a line cycle (=10 ms), using a moving average method with a window frequency of 100 Hz.

C. Experimental Waveforms in Negative-Sequence Reactive-Power Control

Fig. 10 shows the experimental waveforms when the SDBC-based STATCOM was controlled to draw the rated negative-sequence reactive power from the ac mains. Here, the instantaneous real and imaginary power references p^* and q^* [20] were given by[2]

$$p^* = 5\cos(2\omega t + 5\pi/6) \qquad [\mathrm{kW}] \tag{5}$$

$$q^* = 5\sin(2\omega t + 5\pi/6). \qquad [\mathrm{kvai}]. \tag{6}$$

[2]The unit "vai" (volt ampere imaginary) is introduced to the instantaneous imaginary power, according to [21].

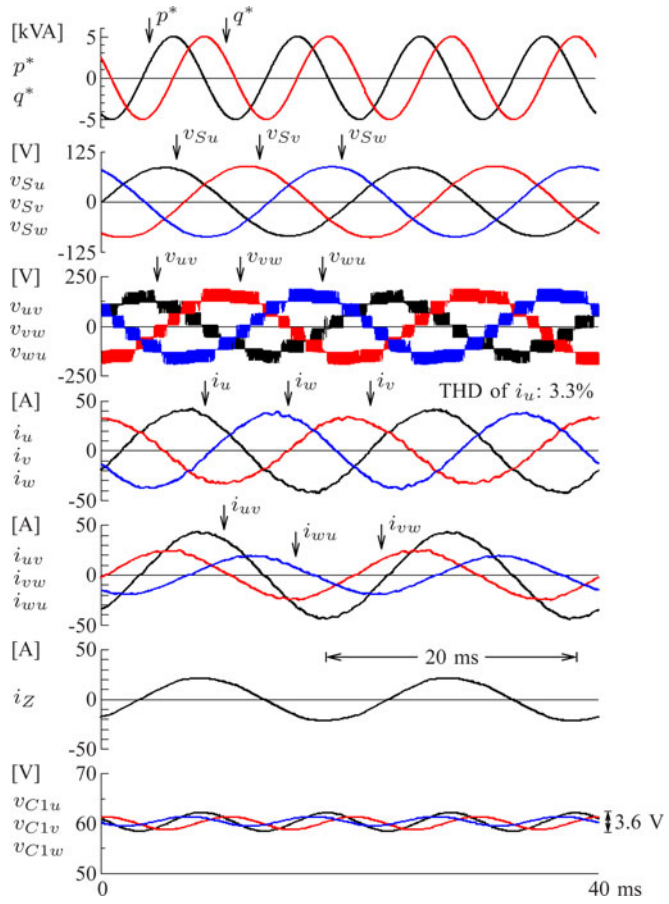

Fig. 10. Experimental waveforms when the SDBC-based STATCOM was controlled to draw the rated negative-sequence reactive power of 5 kV·A from the ac mains.

Note that the initial phase was set intentionally as $5\pi/6$ to make the amplitude of i_{uv} the largest. As a result, i_{uv} is in phase with i_Z, where three-phase line-to-neutral ac mains voltages in Fig. 9 are assumed as

$$v_{Su} = \sqrt{2/3}\,100\sin\omega t \quad [\mathrm{V}] \tag{7}$$

$$v_{Sv} = \sqrt{2/3}\,100\sin(\omega t - 2\pi/3) \quad [\mathrm{V}] \tag{8}$$

$$v_{Sw} = \sqrt{2/3}\,100\sin(\omega t - 4\pi/3) \quad [\mathrm{V}]. \tag{9}$$

The three-phase line current references i_u^*, i_v^*, and i_w^* can be calculated as follows:

$$i_u^* = 41\sin(\omega t - \pi/6) \quad [\mathrm{A}] \tag{10}$$

$$i_v^* = 41\sin(\omega t + \pi/2) \quad [\mathrm{A}] \tag{11}$$

$$i_w^* = 41\sin(\omega t - 5\pi/6) \quad [\mathrm{A}]. \tag{12}$$

The waveforms of v_{uv}, v_{vw}, and v_{wu} at the ac side of the SDBC in Fig. 10 have seven levels of voltage steps as expected, thus resulting in mitigating harmonic voltages and common-mode and differential-mode voltages. When attention is paid to the three-phase line currents, i_u leads i_w by $2\pi/3$, and i_w leads i_v by $2\pi/3$. This means that the three-phase rotating sequence of the line currents is opposite to that of the line-to-neutral voltages. The waveforms of i_u, i_w, and i_v look almost sinusoidal because the total harmonic distortion (THD) value of i_u is 3.3% for example. The amplitudes of i_u, i_w, and i_v are 42, 39, and 35 A, respectively, which are slightly different from their ideal current of 41 A, given by (10)–(12). The reason for the differences came from the overall voltage control making the three clusters draw three-phase imbalanced active powers from the ac mains under the conditions given by (5) and (6).

When attention is paid to the three-phase cluster currents, i_{uv} lags v_{uv} by $\pi/2$, thus indicating that the u-phase cluster operates as an inductor. On the other hand, i_{vw} and i_{wu} lead v_{vw} and v_{wu} by $\pi/2$, respectively, thus suggesting that both v-phase and w-phase clusters act as a capacitor. This difference between the inductive operation and the capacitive operation makes the amplitude of v_{uv} slightly smaller than those of v_{vw} and v_{wu}. As expected, the circulating current i_Z is in phase with i_{uv}. Therefore, i_{uv} gets the largest in amplitude among the three. The switching ripple contained in i_Z is negligible because the three ac inductors present $3L_{\mathrm{ac}}$ (=18%) to the circulating current. The waveforms of dc capacitor voltages v_{C1u}, v_{C1v}, and v_{C1w} exhibit that their dc mean voltages are well regulated at their voltage reference of 60 V.

D. Experimental Waveforms in Complex Power Control

Fig. 11 shows the experimental waveforms when the SDBC-based STATCOM was controlled to draw from the ac mains an active power fluctuating at 10 Hz, a positive-sequence reactive (capacitive) power and a negative-sequence reactive power with the same amplitude as 1.7 kW or 1.7 kvai. To do so, the instantaneous real and imaginary power references p^* and q^* were given as follows:

$$p^* = 1.7\sin(\omega t/5) + 1.7\cos(2\omega t + 5\pi/6) \quad [\mathrm{kW}] \tag{13}$$

$$q^* = -1.7 + 1.7\sin(2\omega t + 5\pi/6). \quad [\mathrm{kvai}]. \tag{14}$$

The waveforms of the three-phase line currents i_u, i_v, and i_w, and the three-phase cluster current i_{uv}, i_{vw}, and i_{wu} in Fig. 11 reveal that their amplitudes and phases vary dynamically time by time. However, the amplitude of i_Z is proportional only to the amplitude of negative-sequence reactive power. This consideration is confirmed by the fact that the amplitude of i_Z in Fig. 11 is one-third of that in Fig. 10 because the amplitude of negative-sequence reactive power in Fig. 11 is one-third of that in Fig. 10.

Each of the dc capacitor voltages v_{C1u}, v_{C1v}, and v_{C1w} in Fig. 11 includes 10-Hz and 100-Hz components. The 10-Hz component is caused by the active power fluctuating at 10 Hz, while the 100-Hz component comes from the negative-sequence reactive power including such an instantaneous real power fluctuating at 100-Hz as shown in (13). It is clear from Fig. 11 that the amplitude of the 10-Hz component is much larger than that of the 100-Hz component. It is well known that the amplitude of an ac component contained in the dc capacitor voltage is inversely proportional to the frequency of the ac component as long as the amplitude of active power is the same as that of negative-sequence reactive power. However, positive-sequence reactive power produces no effect on the dc capacitor voltages.

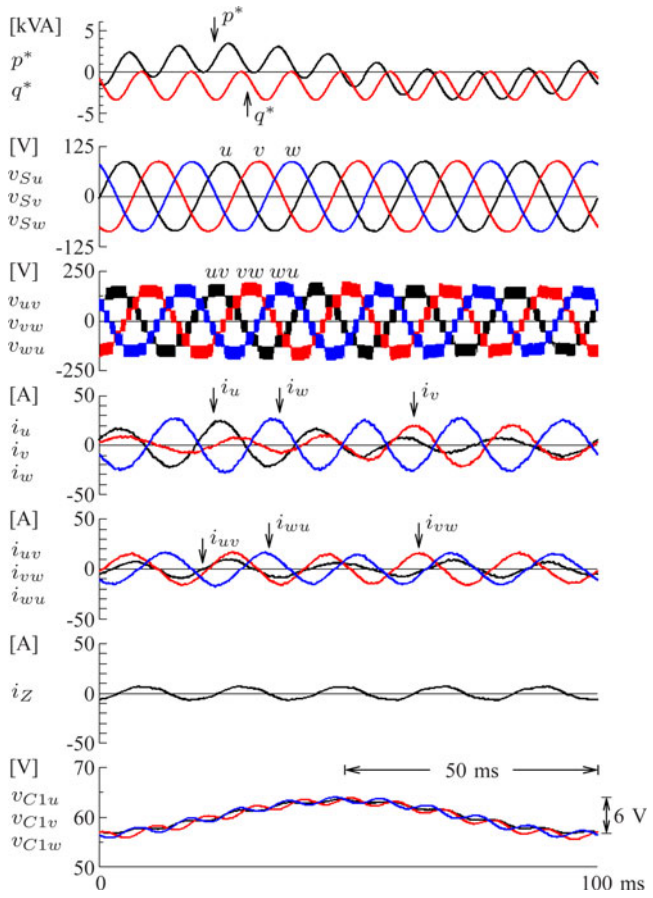

Fig. 11. Experimental waveforms when the SDBC-based STATCOM was controlled to draw from the ac mains a positive-sequence reactive power of 1.7 kV·A, a negative-sequence reactive power of 1.7 kV·A, and a fluctuating (10 Hz) active power together.

The dc mean voltages of v_{C1u}, v_{C1v}, and v_{C1w} over a time of 100 ms are well regulated at their voltage reference of 60 V.

VI. Application of the DSCC to a Motor Drive

The DSCC is applicable not only to HVDC and BTB systems in power transmission systems but also to medium-voltage motor drives. However, it would be impractical to apply the DSCC to, for example, a steel mill drive that requires the rated torque as well as a transient overtorque, say 150%–200% torque, in a low-speed region. Thus, this section describes a DSCC-based motor drive for fans, blowers, and compressors, the torque of which is proportional to a square of rotating speed.

A. Circuit Configuration

Fig. 12(a) shows the circuit configuration of the DSCC for a motor drive [22], [23]. Each leg consists of a stack of eight bidirectional chopper-cells depicted in Fig. 12(b), and a coupled or center-tapped inductor in Fig. 12(c). Fig. 12(a) produces 9-level (17-level in line-to-line) PWM waveforms since the number of chopper cell per leg is eight. The terminals of the coupled inductor, "*a*" and "*b*" are connected to the positive and negative arms, and the center tap "*c*" is directly connected to the motor.

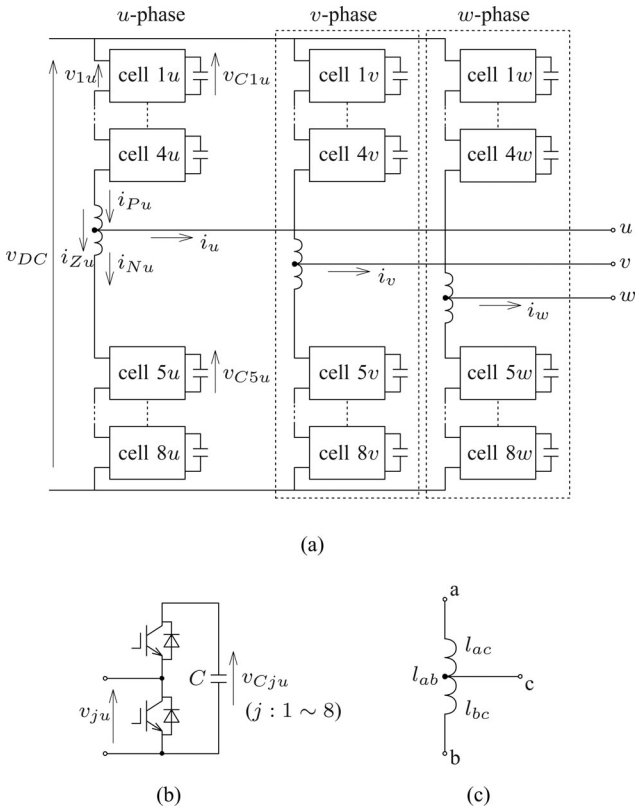

Fig. 12. Circuit configuration of the DSCC with eight cells per leg for experiment. (a) Power circuit. (b) Chopper-cell. (c) Coupled or center-tapped inductor.

The following equation exists in Fig. 12(c):

$$l_{ab} = 4l_{ac} = 4l_{bc}. \tag{15}$$

When attention is paid to the u-phase currents in Fig. 12(a), i_{Pu} and i_{Nu} are the positive and negative arm currents, i_u is the motor current, and i_{Zu} is the circulating current between the dc input and the leg [22]. The following equations exist among the four u-phase currents:

$$i_{Pu} = \frac{i_u}{2} + i_{Zu} \tag{16}$$

$$i_{Nu} = -\frac{i_u}{2} + i_{Zu} \tag{17}$$

$$i_{Zu} = \frac{1}{2}(i_{Pu} + i_{Nu}). \tag{18}$$

The first terms of the right-hand side in (16) and (17), $i_u/2$ and $-i_u/2$ are out of phase by 180° with respect to each other. This means that the magnetic fluxes produced by these current components cancel out each other. As a result, the coupled inductor presents the inductance l_{ab} only to the circulating current i_{Zu}, and no inductance to the motor current i_u. Moreover, the single coupled inductor is smaller in size and lighter in weight than the two noncoupled inductors shown in Fig. 3(b). Thus, Fig. 3(a) is preferable to Fig. 3(b) in terms of applying the DSCC to motor drives.

The three circulating currents i_{Zu}, i_{Zv}, and i_{Zw} are independent of each other because the dc terminals of a three-phase diode rectifier are connected to the dc terminals of the DSCC. Hence, the following pays attention to the u-phase because the operating principle is identical among the three legs.

B. Mean-Voltage Control of Floating DC Capacitors

Mean-voltage control of eight floating dc capacitors per leg in Fig. 12(a) can be divided into averaging control and balancing control. The aim of this mean-voltage control is to regulate, not the "instantaneous" voltage, but the dc "mean" voltage to its reference. The averaging control forces the u-phase average voltage $\bar{v}_{Cu}$ to follow its reference v_C^*, where $\bar{v}_{Cu}$ is given by[3]

$$\bar{v}_{Cu} = \frac{1}{8}\sum_{j=1}^{8} v_{Cju}. \tag{19}$$

This averaging control includes a current-minor-loop controller for the circulating current [22].

The balancing control can be used with the following motor-voltage reference v_u^*.

$$v_u^* = \sqrt{\frac{2}{3}} V \sin 2\pi f t. \tag{20}$$

Here, V is the motor line-to-line rms voltage, and f is the inverter frequency. Note that v_u^* refers to the motor line-to-neutral voltage reference. The voltage reference obtained from the balancing control, v_{Bju}^* for $j = 1-4$ is represented as follows:

$$v_{Bju}^* = K(v_C^* - v_{Cju})v_u^* \tag{21}$$

and v_{Bju}^* for $j = 5-8$ as

$$v_{Bju}^* = -K(v_C^* - v_{Cju})v_u^*. \tag{22}$$

Note that v_{Bju}^* contains an inverter-frequency component forming an active power with that of i_{Pu} or i_{Nu}.

The positive-arm and negative-arm voltage references of each chopper cell, v_{ju}^* are given by

$$v_{ju}^* = v_{Au}^* + v_{Bju}^* - \frac{v_u^*}{4} + \frac{v_{\rm dc}}{8} \quad (j: 1-4) \tag{23}$$

$$v_{ju}^* = v_{Au}^* + v_{Bju}^* + \frac{v_u^*}{4} + \frac{v_{\rm dc}}{8} \quad (j: 5-8) \tag{24}$$

where v_{Au}^* is the voltage reference obtained from the averaging control. The last term of the right-hand side in (23) and (24), $v_{\rm dc}/8$ corresponds to a feedforward control of the dc-link voltage $v_{\rm dc}$. The voltage reference v_{ju}^* is normalized by each dc-capacitor voltage v_{Cju}. Then, it is compared with a triangular carrier waveform, the value of which in a range of 0 to 1, with a PWM carrier frequency of 1 kHz. In [22] and [23], a detailed explanation of the averaging and balancing control methods including their control block diagrams is given.

[3]The subscript symbol j means the numbering of eight chopper cells.

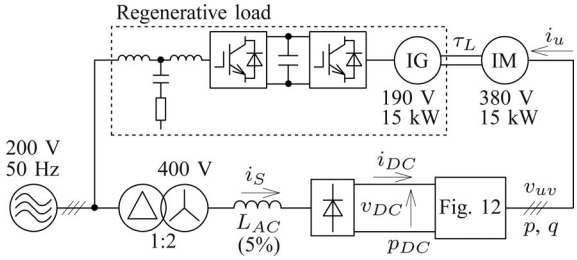

Fig. 13. 400-V, 15-kW experimental system based on the DSCC without dc-link capacitor.

TABLE IV
CIRCUIT PARAMETERS FOR THE EXPERIMENTAL SYSTEM BASED ON THE DSCC

Nominal line-to-line rms voltage	V_S	400 V
Power rating	P	15 kW
AC inductor	L_{AC}	1.75 mH (5.0%)
Nominal dc-link voltage	V_{DC}	540 V
Coupled inductor	l_{ab}	4.0 mH (12%)
DC capacitor of chopper-cell	C	3.3 mF
DC capacitor voltage reference	V_C^*	140 V
Unit capacitance constant [19]	H	52 ms
PWM carrier frequency		1 kHz
Equivalent carrier frequency		8 kHz

Values in ( ) are on a three-phase, 400-V, 15-kW, 50-Hz base.

TABLE V
SPECIFICATIONS OF THE 380-V, 15-KW INDUCTION MOTOR

Rated output power	15 kW
Rated line-to-line rms voltage	380 V
Rated frequency	50 Hz
Rated line rms current	32 A
Pole-pair number	2
Moment of inertia	0.2 kg·m^2

C. Experimental System Configuration

Fig. 13 shows the experimental system configuration of the 400-V, 15-kW downscaled system. Table IV summarizes the circuit parameters used for experiment. Note that no common dc-link capacitor is connected between the diode rectifier and the DSCC although a dc voltage sensor is installed to detect the dc-link voltage. This is a significant difference in experimental system configuration between this present paper and the previous paper [23]. Generally, adjustable-speed motor drives for fans and blowers require neither regenerative braking nor fast speed control, thus resulting in eliminating the common dc-link capacitor from Fig. 13. This elimination is of great advantage to such a medium-voltage motor drive because no dc-link capacitor would cause any rush current if a short circuit occurred across the common dc link.

A fully digital controller using a DSP and multiple FPGAs has set a dead time of each gate signal as 4 μs, and a dc-voltage reference of each chopper cell as 140 V. The ac output terminals of the inverter are directly connected to an induction motor rated at 380 V and 15 kW. Table V summarizes specifications of the induction motor. A regenerative load in Fig. 13 consists of an induction generator rated at 190 V and 15 kW, and two PWM converters connected BTB. The so-called vector control or field-oriented control is applied to the induction generator,

which enables one to load an arbitrary instantaneous torque τ_L on the induction motor.

D. Experimental Waveforms

Fig. 14 shows experimental waveforms in a steady-state condition when the inverter frequency was 50 Hz and the load torque was equal to the rated motor torque. The waveforms were sampled and held at a sampling frequency of 500 kHz. The motor line-to-line voltage v_{uv} is a 15-level PWM waveform with voltage steps as low as 70 V where the chopper-cell modulation index is 0.93. As a consequence, v_{uv} contains much less harmonic voltage as well as much less common-mode voltage than a traditional two-level voltage-source PWM inverter. This results in significantly reducing electromagnetic interference (EMI) emissions, ground leakage current, bearing current, and so on. Since the carrier frequency of each chopper cell is 1 kHz, the equivalent switching frequency of the inverter is 8 kHz (=1 kHz $\times$ 8).

The three-phase motor-side ac currents i_u, i_v, and i_w are sinusoidal and balanced with a fundamental component of 50 Hz, so that motor-torque ripple can be mitigated. The 4-kHz switching-ripple component included in i_{Pu} and i_{Nu} depends on the inductance value of the coupled inductor l_{ab}.

The dc capacitor voltage v_{C1u} contains both dc and ac components as shown in Fig. 14, in which the mean-voltage control regulates the dc component at 140 V. The ac components consist of a dominant fundamental (50 Hz) component, and a second-order (100 Hz) harmonic component. The ac components included in v_{C1u} are equal to those in v_{C2u}, v_{C3u}, and v_{C4u} because the chopper cells numbered 1 to 4 carry the common arm current i_{Pu} under the same duty ratio.[4] In the same way, the ac components included in v_{C5u} are equal to those in v_{C6u}, v_{C7u}, and v_{C8u}. Each of the arm currents i_{Pu} and i_{Nu} contains an amount of second-order harmonic current as a result of achieving the mean-voltage control of eight floating dc capacitors per leg. However, no second-order harmonic current appears in i_u because those included in i_{Pu} and i_{Nu} are in phase and the same in amplitude.

The waveform of the supply-side ac current i_{Su} is similar to that when only a resistive load is connected on the dc side of a three-phase diode rectifier without dc-link capacitor. It is well known that the waveform of i_{Su} cannot comply with harmonic guidelines or regulations. A transformerless hybrid active filter for a medium-voltage motor drive has been proposed, and its viability and effectiveness have been confirmed by a downscaled experimental system. It devotes itself to the three-phase six-pulse diode rectifier used as the front end of such a medium-voltage motor drive. The hybrid filter is characterized by direct connection of a simple *LC* filter tuned to the seventh-harmonic frequency with a small-rated active filter using a three-level diode-clamped PWM converter in series [24].

[4]The duty ratio is defined by the ratio of the time-varying on-duration to the switching period.

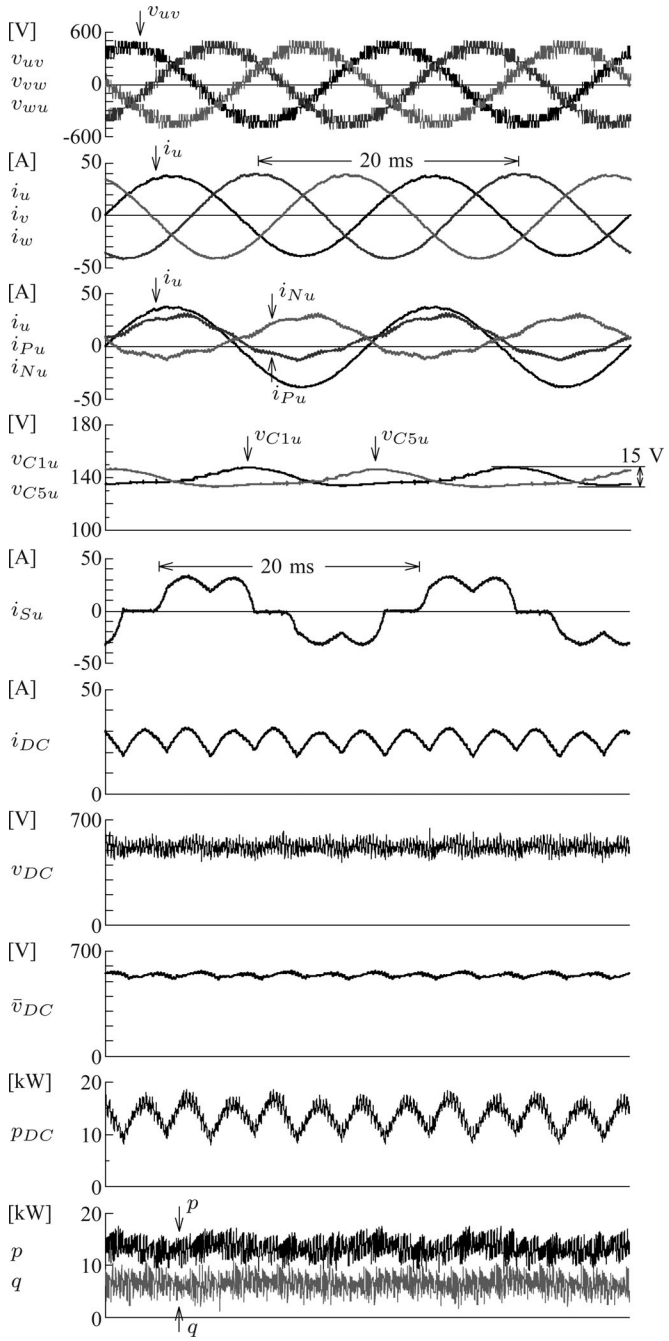

Fig. 14. Experimental waveforms from the DSCC when the inverter frequency was 50 Hz and the load torque was the rated motor torque.

E. Instantaneous Real and Imaginary Powers at the DC and AC Sides

Fig. 14 presents the waveforms of the instantaneous real power p and the instantaneous imaginary power q at the ac side of the DSCC, that is, at the motor terminals. The waveform of instantaneous real power $p_{\rm dc}$ at the dc side is given by

$$p_{\rm dc} = v_{\rm dc} \times i_{\rm dc} \tag{25}$$

where $v_{\rm dc}$ is the dc-link voltage, and $i_{\rm dc}$ is the dc current flowing through the dc link. Note that no instantaneous imaginary power

exists at the dc side of the inverter. The waveform of $\bar{v}_{\rm dc}$ in Fig. 14 is observed from $v_{\rm dc}$ through a first-order low-pass filter with a cutoff frequency of 1 kHz. The waveform of p is different from that of $p_{\rm dc}$ because the DSCC has the 24 floating dc capacitors acting as energy storage elements. However, the dc mean component of p would be equal to that of $p_{\rm dc}$ if the DSCC produced no loss.

F. Which is Better, the DSCC and a Multilevel Diode-Clamped Inverter?

A serious question may be asked "Which is better, the DSCC or a multilevel diode-clamped inverter for medium-voltage motor drives?" It is not easy to answer the question because the general answer would depend on design and cost issues including nominal grid voltages, motor voltage and current ratings, applications, power switching devices available, and so on.

Although the DSCC has no practical limitation on the converter-cell count per arm due to modular structure, the diode-clamped inverter has a practical limitation on the voltage level. Since the three-level neutral-point-clamped (diode-clamped) inverter was invented at the end of the 1970s [25], it has been put into practical use, not only as a general-purpose PWM inverter, but also for a steel mill drive, the Japanese bullet train the "Shinkansen," the unified power flow controller, and so on [26]. However, among multilevel diode-clamped inverters with a voltage level more than three, only the five-level inverter would be a good candidate competing with the DSCC from a practical point of view [27]–[33]. The main reasons are that multilevel diode-clamped inverters with a voltage level more than five would suffer from voltage imbalance among split dc capacitors on the dc link, and that the number of the clamping diodes required increases significantly as the voltage level increases.

On the other hand, it would be difficult to apply the DSCC to the motor drive requiring the rated torque in a low-speed region. Thus, the DSCC would confine its application to medium-voltage motor drives for fans, blowers, and compressors, the torque of which is proportional to a square of motor speed. However, the five-level diode-clamped inverter has no limitation on its applications.

VII. Conclusion

This paper has described the MMCC family with focus on classification, terminology, and application. The converter family is characterized by cascade connection of modular chopper-cells or bridge-cells to form each cluster or arm. This brings flexibility to circuit design, and results in low-voltage steps. Moreover, this paper has exhibited multiple applications of the MMCC family to grid connections and motor drives. Experimental results obtained from three downscaled systems have confirmed that the MMCC family with low-voltage steps has shown significant promise as environment-friendly medium-voltage high-power converters in terms of low-voltage/current harmonics and low EMI emissions.

Among the four MMCC family members, the SSBC is the most promising as a BESS for positive-sequence active-power control and as a STATCOM for positive-sequence reactive-power control with the lowest converter-cell count. The SDBC may confine its application to a STATCOM for negative-sequence reactive-power control because the converter-cell count of SDBC is $\sqrt{3}$ times of that of the SSBC. The DSCC is expected to fill the role of power conversion in the next-generation multiterminal HVDC and BTB systems as well as medium-voltage motor drives. The DSBC is characterized by having buck and boost functions in addition to rectification and inversion although it requires a large number of power switching devices.

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References

[1] P. W. Hammond, "A new approach to enhance power quality for medium voltage ac drives," *IEEE Trans. Ind. Appl.*, vol. 33, no. 1, pp. 202–208, Jan./Feb. 1997.

[2] M. Marchesoni, M. Mazzucchelli, and S. Tenconi, "A noncoventional power converter for plasma stabilization," *IEEE Trans. Power Electron.*, vol. 5, no. 2, pp. 212–219, Apr. 1990.

[3] M. Marchesoni and M. Mazzucchelli, "Multilevel converters for high power ac drives: A review," in *Conf. Rec. IEEE Int. Symp. Ind. Electron.*, 1993, pp. 38–43.

[4] J. S. Lai and F. Z. Peng, "Multilevel converters–A new breed of power converters," *IEEE Trans. Ind. Appl.*, vol. 32, no. 3, pp. 509–517, May/Jun. 1996.

[5] F. Z. Peng, J. S. Lai, J. W. McKeever, and J. VanCoevering, "A multilevel voltage-source inverter with separate dc sources for static VAr generation," *IEEE Trans. Ind. Appl.*, vol. 32, no. 5, pp. 1130–1138, Sep./Oct. 1996.

[6] L. M. Tolbert, F. Z. Peng, and T. G. Habetler, "Multilevel converters for large electric drives," *IEEE Trans. Ind. Appl.*, vol. 35, no. 1, pp. 36–44, Jan./Feb. 1999.

[7] R. Marquardt and A. Lesnicar, "A new modular voltage source inverter topology," in *Conf. Rec. Eur. Conf. Power Electron. Appl.*, 2003, pp. 1–10. [CD-ROM].

[8] M. Glinka and R. Marquardt, "A new single-phase ac/ac-multilevel converter for traction vehicles operating on ac line voltage," in *Conf. Rec. Eur. Conf. Power Electron. Appl.*, 2003, pp. 1–10. [CD-ROM].

[9] A. Alesina and M. Venturini, "Solid-state power conversion: A Fourier analysis approach to generalized transformer synthesis," *IEEE Trans. Circ. Syst.*, vol. 28, no. 4, pp. 319–330, Apr. 1981.

[10] (2007). [Online]. Available: http://www.modernpowersystems.com

[11] S. Allebrod, R. Hamerski, and R. Marquardt, "New transformerless, scalable modular multilevel converters for HVDC-transmission," in *Conf. Rec. IEEE Power Electronics Spec. Conf.*, 2008, pp. 174–179.

[12] H. Akagi, "Classification, terminology, and application of the modular multilevel cascade converter (MMCC)," in *Conf. Rec. Int. Power Electron. Conf.-Sappro/ECCE-Asia*, 2010, pp. 508–515.

[13] S. Inoue and H. Akagi, "A bidirectional isolated dc-dc converter as a core circuit of the next-generation medium-voltage power conversion system," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 535–542, Mar. 2007.

[14] H. Akagi, S. Inoue, and T. Yoshii, "Control and performance of a transformerless cascade PWM STATCOM with star configuration," *IEEE Trans. Ind. Appl.*, vol. 43, no. 4, pp. 1041–1049, Jul./Aug. 2007.

[15] L. Maharjan, S. Inoue, H. Akagi, and J. Asakura, "SOC (state-of-charge)-balancing control of a battery energy storage system based on a cascade PWM converter," *IEEE Trans. Power Electron.*, vol. 24, no. 6, pp. 1628–1636, Jun. 2009.

[16] L. Maharjan, T. Yamagishi, H. Akagi, and J. Asakura, "Fault-tolerant operation of a battery energy storage system based on a multilevel cascade PWM converter with star configuration," *IEEE Trans. Power Electron.*, vol. 25, no. 9, pp. 2386–2396, Sep. 2010.

[17] L. Maharjan, T. Yamagishi, and H. Akagi, "Active-power control of individual converter cells of a battery energy storage system based on a

multilevel cascade PWM converter," *IEEE Trans. Power Electron.*, to be published in May/Jun. 2011.
[18] K. Fujii, U. Schwarzer, and R. W. De Doncker, "Comparison of hard-switched multi-level inverter topologies for STATCOM by loss-implemented simulation and cost estimation," in *Conf. Rec. IEEE Power Electron. Spec. Conf.*, 2005, pp. 340–346.
[19] H. Fujita, S. Tominaga, and H. Akagi, "Analysis and design of a dc voltage-controlled static VAr compensator using quad-series voltage-source inverters," *IEEE Trans. Ind. Applicat.*, vol. 32, no. 4, pp. 970–977, Jul./Aug. 1996.
[20] H. Akagi, Y. Kanazawa, and A. Nabae, "Instantaneous reactive power compensators comprising switching devices without energy storage components," *IEEE Trans. Ind. Appl.*, vol. IA-20, no. 3, pp. 625–630, May/Jun. 1984.
[21] H. Akagi, E. H. Watanabe, and M Aredes, *Instantaneous Power Theory and Applications to Power Conditioning*. Piscataway, NJ: IEEE Press, 2007.
[22] M. Hagiwara and H. Akagi, "Control and experiment of pulsewidth-modulated modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 24, no. 7, pp. 1737–1746, Jul. 2009.
[23] M. Hagiwara, K. Nishimura, and H. Akagi, "A medium-voltage motor drive with a modular multilevel PWM inverter," *IEEE Trans. Power Electron.*, vol. 25, no. 7, pp. 1786–1799, Jul. 2010.
[24] H. Akagi and R. Kondo, "A transformerless hybrid active filter using a three-level pulsewidth modulation (PWM) converter for a medium-voltage motor drive," *IEEE Trans. Power Electron.*, vol. 25, no. 6, pp. 1365–1374, Jun. 2010.
[25] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Trans. Ind. Applicat.*, vol. IA-17, no. 5, pp. 518–523, Sep./Oct. 1981.
[26] B. Wu, *High-Power Converters and AC Drives*. Piscataway, NJ: IEEE Press, 2006.
[27] R. W. Menzies, P. Steimer, and J. K. Steinke, "Five-level GTO inverters for large induction motor drives," *IEEE Trans. Ind. Appl.*, vol. 30, no. 4, pp. 938–944, Jul./Aug. 1994.
[28] M. Saeedifard, R. Iravani, and J. Pou, "Analysis and control of dc-capacitor-voltage-drift phenomenon of a passive front-end five-level converter," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 3255–3236, Dec. 2007.
[29] S. Busquets-Monge, S. Alepuz, J. Rocabert, and J. Bordonau, "Pulsewidth modulations for the comprehensive capacitor voltage balance of n-level three-leg diode-clamped converters," *IEEE Trans. Power Electron.*, vol. 24, no. 5, pp. 1364–1375, May 2009.
[30] Z. Pan and F. Z. Peng, "A sinusoidal PWM method with voltage balancing capability for diode-clamped five-level converters," *IEEE Trans. Ind. Appl.*, vol. 45, no. 63, pp. 1028–1034, May/Jun. 2009.
[31] N. Hatti, Y. Kondo, and H. Akagi, "Five-level diode-clamped PWM converter connected back-to-back for motor drives," *IEEE Trans. Ind. Appl.*, vol. 44, no. 4, pp. 1268–1276, Jul./Aug. 2008.
[32] N. Hatti, K. Hasegawa, and H. Akagi, "A 6.6-kV transformerless motor drive using a five-level diode-clamped PWM inverter for energy savings of pumps and blowers," *IEEE Trans. Power Electron.*, vol. 24, no. 3, pp. 796–803, Mar. 2009.
[33] K. Hasegawa and H. Akagi, "A new dc-voltage-balancing circuit including a single coupled inductor for a five-level diode-clamped PWM inverter," *IEEE Trans. Ind. Appl.*, vol. 47, no. 2, pp. 841–852, Mar./Apr. 2011.

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