XTX™ Specification Revision 1.2

XTX™ Pinout, signal description and implementation guidelines

XTX™ Specification

Revision 1.2

Revision History

Revision	Date	Author	Revision History
1.0	July 13, 05	congatec AG/MAREKMICRO GmbH	Initial release
1.0a	June 8, 06	XTX™ Consortium	Added information from XTX-Spec-Errata10. Changed format of document.
1.1	July 11, 06	XTX™ Consortium	Added additional information about connectors X1, X3, and X4.
1.2	Dec. 5, 06	XTX™ Consortium	Added pin 60 PP_TPM to table 2 and X2 connector schematic. Added description for PP_TPM to table 16. Added Hirose connector location peg hole tolerances note to section 1.3.1.

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Preface

ETX® Concept and XTX™ Extension

The ETX® concept is an off the shelf, multi vendor, Single-Board-Computer that integrates all the core components of a common PC and is mounted onto an application specific carrier board. ETX® modules have a standardized form factor of 95mm x 114mm and have specified pinouts on the four system connectors that remain the same regardless of the vendor. The ETX® module provides most of the functional requirements for any application. These functions include, but are not limited to, graphics, sound, keyboard/mouse, IDE, Ethernet, parallel, serial and USB ports. Four ruggedized connectors provide the carrier board interface and carry all the I/O signals to and from the ETX® module.

Carrier board designers can utilize as little or as many of the I/O interfaces as deemed necessary. The carrier board can therefore provide all the interface connectors required to attach the system to the application specific peripherals. This versatility allows the designer to create a dense and optimized package, which results in a more reliable product while simplifying system integration. Most importantly ETX® applications are scalable, which means once a product has been created there is the ability to diversify the product range through the use of different performance class ETX® modules. Simply unplug one module and replace it with another, no redesign is necessary.

XTX™ is an expansion and continuation of the well-established and highly successful ETX® standard. XTX™ offers the newest I/O technologies on this proven form factor. Now that the ISA bus is being used less and less in modern embedded applications the XTX™ standard offers an array of different features on the X2 connector than those currently found on the ETX® platform. These features include new serial high speed buses such as PCI Express™ and Serial ATA®. All other signals found on connectors X1, X3, and X4 remain the same in accordance to the ETX® standard and therefore will be completely compatible. If the embedded PC application still requires the ISA bus then an ISA bridge can be implemented on the application specific carrier board or the readily available LPC bus located on the XTX™ module may be used.

XTX™ is an ETX(R) Component SBC Specification extension.

XTX™ is fully compliant to ETX(R) Specification except for the X2 [ISA bus] connector signal definition.

The ISA bus signals on the X2 connector are replaced by state of the art interface technologies such as:

- PCIexpress™
- ExpressCard™
- SATA
- USB
- Digital Audio
- LPC interface

Plus additional control signals.

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Disclaimer

The information contained within this XTX™ Specification, including but not limited to any product specification, is subject to change without notice.

The XTX™ Consortium provides no warranty with regard to this XTX™ Specification or any other information contained herein and hereby expressly disclaims any implied warranties of merchantability or fitness for any particular purpose with regard to any of the foregoing. The XTX™ Consortium assumes no liability for any damages incurred directly or indirectly from any technical or typographical errors or omissions contained herein or for discrepancies between the product and the XTX™ interface specification. In no event shall the XTX™ Consortium be liable for any incidental, consequential, special, or exemplary damages, whether based on tort, contract or otherwise, arising out of or in connection with this XTX™ interface specification or any other information contained herein or the use thereof.

Intended Audience

This XTX™ interface specification is intended for technically qualified personnel. It is not intended for general audiences.

Symbols

The following symbols may be used in this specification:

Warning

Warnings indicate conditions that, if not observed, can cause personal injury.

Caution

Cautions warn the user about how to prevent damage to hardware or loss of data.

Note

Notes call attention to important information that should be observed.

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XTX™ Logo usage

The XTX™ logo is freely available for members of the XTX™ consortium. The logo can only be applied to products which are fully compliant to the latest specification of the XTX™ Standard.

High resolution formats are available at the members area www.xtx-standard.org.

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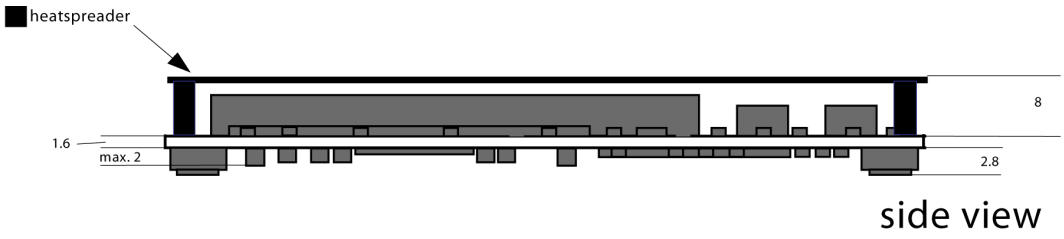
Contents

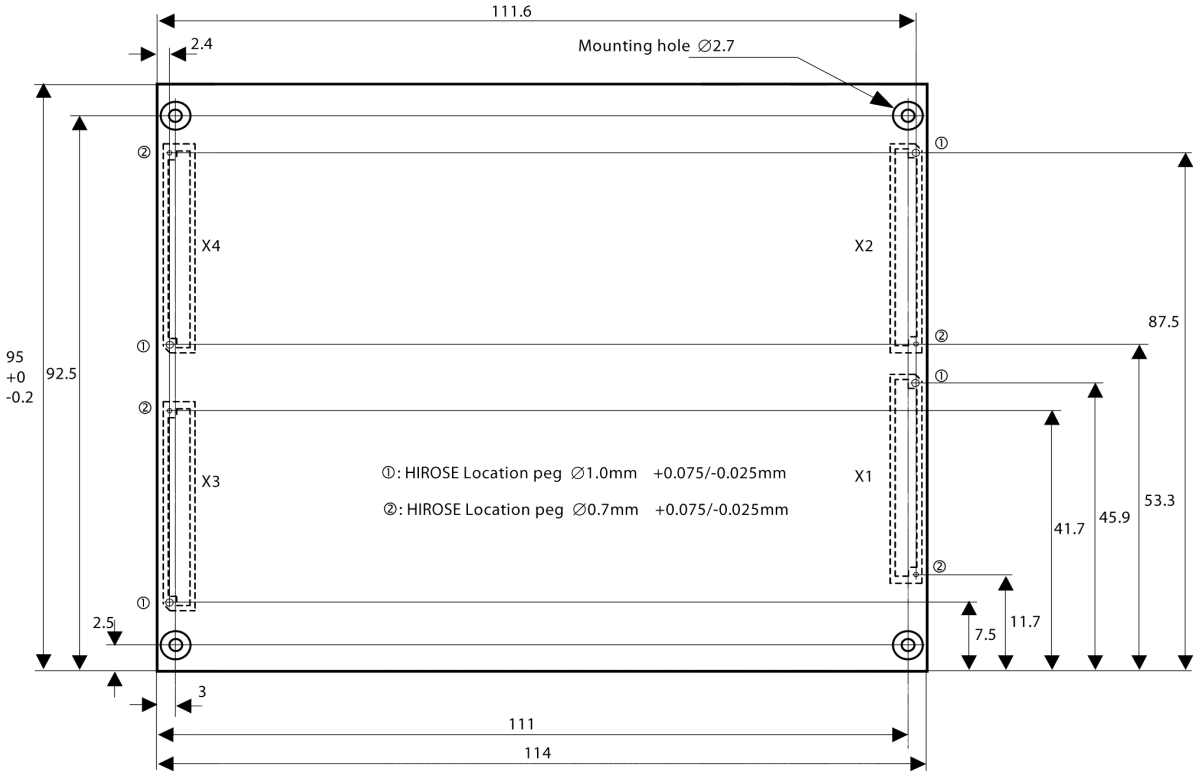
1 Connector Locations

XTX™ modules have four connectors that provide all the signals required for building customized embedded applications. The mechanical drawing below shows the connector locations and overall dimensions of an XTX™ module including heatspreader.

1.1 Mechanical Drawing



side view



top view

1.2 XTX™ Mechanical Characteristics

The XTX™ module, including the heatspreader plate, is up to approximately 12 mm thick. The components located on the top of the module are up to 8 mm high. The bottom components are a maximum of 2 mm high while the connectors X1 to X4 (FX8-100P-SV) on the XTX™ module are 2.8mm high. These will be connected to their counterpart receptacles (FX8-100S) on the Carrier Board. Refer to section 1.3 regarding FX8-100S receptacle specifications.

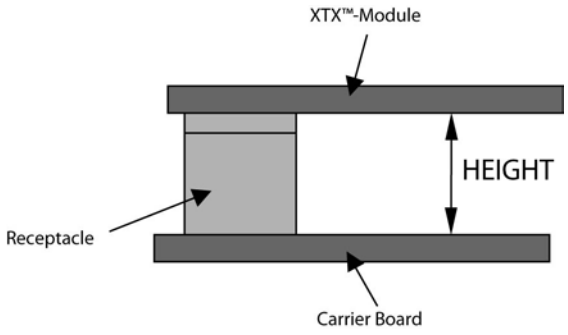
The heatspreader offered for XTX™ modules acts as a thermal coupling device and is not a heat sink. Heat dissipation devices such as a heat sink with fan or heat pipe may need to be connected to the heatspreader. The dissipation of heat will fluctuate between different CPU boards. Refer to the XTX™ module's manual for heatspreader dimensions and specifications.

1.3 Specification of Receptacles FX8-100S

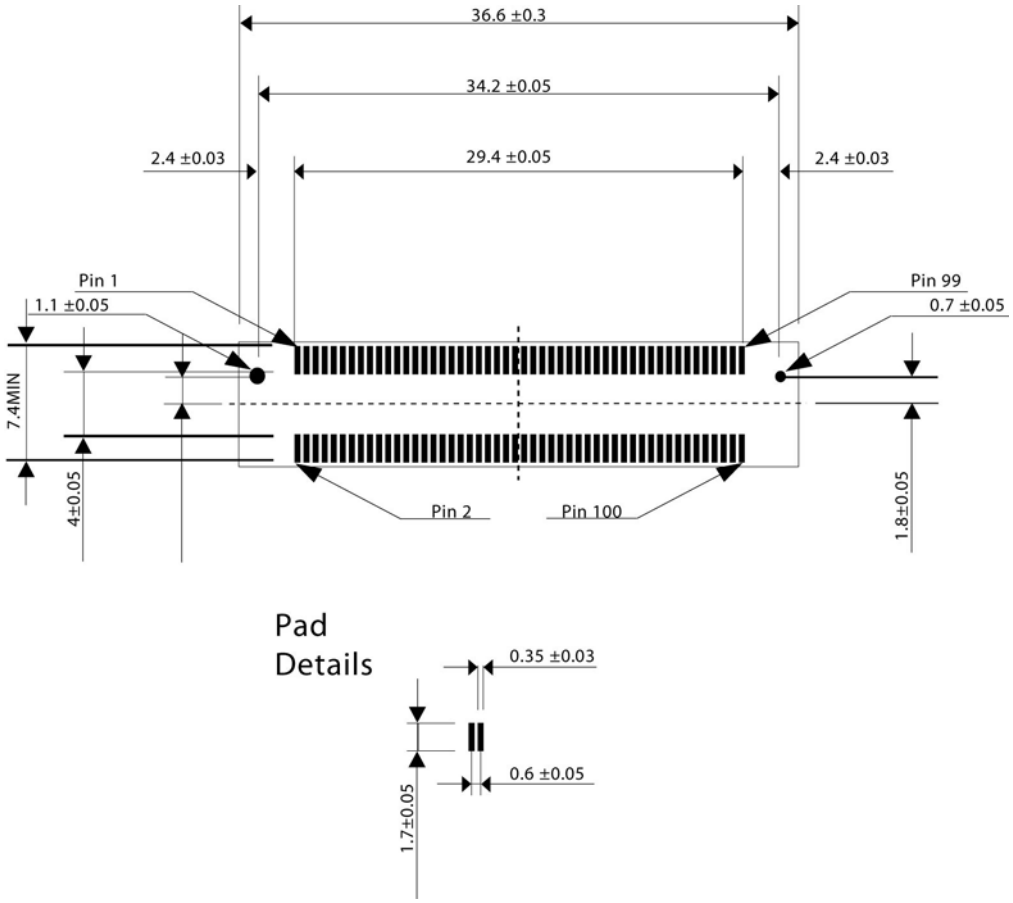
The receptacles for XTX™ module connection allow the base to be stacked to different heights. The following table provides details about the stacking height available.

Manufacturer	Part Number	Specification	Resulting height between carrier board and XTX™ module
HIROSE	FX8-100S-SV	3 + 0.3/-0.2 mm	3.0 + 0.3/-0.2 mm
HIROSE	FX8C-100S-SV5	9.5+0.3/-0.2 mm	9.5+0.3/-0.2 mm

Item	Specification
Current capacity	0.4 A per pin
Rated voltage	100 V AC
Insulation resistance	10 ohms or greater @ 250 V DC
Withstand voltage	300V AC r.m.s.
Contact resistance	45m ohms or less @ 100 mA DC
Contacts	Phosphor bronze (Contacts and leads gold plated)
Insulation	PPS resin (Light brown, UL94V-0)



1.3.1 Footprint of FX8(C)-100S-SV(5) Receptacles



Note

The XTX™ consortium strongly recommends to use the following location peg hole tolerances instead of those indicated in the Hirose footprint drawing above:

- *1.0mm +0.075/-0.025*
- *0.7mm +0.075/-0.025*

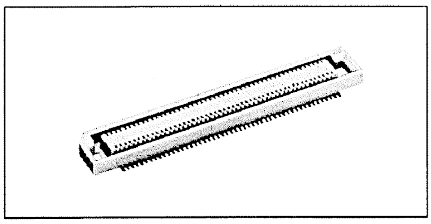
1.3.2 HIROSE FX8 and FX8C Series Information

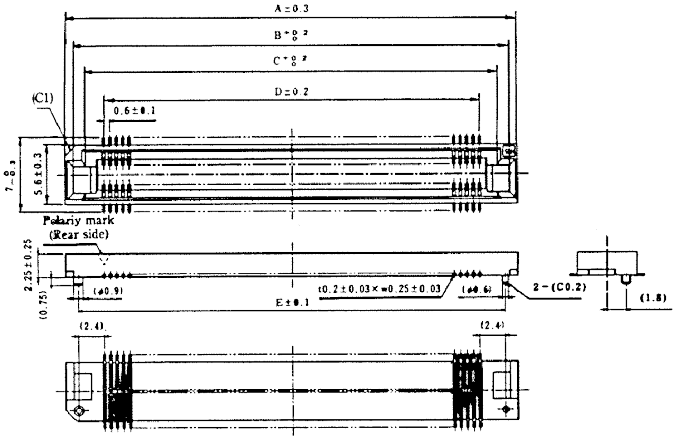
HIROSE designed the FX8 and FX8C connectors especially for the ETX®/XTX™ form factor products. Different contact lengths were utilized to achieve different stacking heights while maintaining the same mating faces. For XTX™ module mating, only FX8 or FX8C connectors should be used.

These connectors have been fully tested on XTX™ applications. When fixed with screws or bolts, all mechanical stability and PCB interference was verified as acceptable. All dimensions and tolerances of the stand-offs were designed to match the XTX™ Specification.

FX8-100S-SV Series Datasheet Excerpt

[FX8-※※S-SV]





Unit: mm

HRS No.	Product No.	Number of Contacts	A	B	C	D	E	Tube Packaging Quantity (pcs)
CL578-0201-5-※※	FX8-60S-SV (※※)	60	24.60	23.05	20.80	17.40	22.20	21
CL578-0203-0-※※	FX8-80S-SV (※※)	80	30.60	29.05	26.80	23.40	28.20	17
CL578-0204-3-※※	FX8-90S-SV (※※)	90	33.60	32.05	29.80	26.40	31.20	15
CL578-0205-6-※※	FX8-100S-SV (※※)	100	36.60	35.05	32.80	29.40	34.20	14
CL578-0206-9-※※	FX8-120S-SV (※※)	120	42.60	41.05	38.80	35.40	40.20	12
CL578-0207-1-※※	FX8-140S-SV (※※)	140	48.60	47.05	44.80	41.40	46.20	10

※※ Blank: Tray packaging 21: Tube packaging 22: Embossed tape packaging

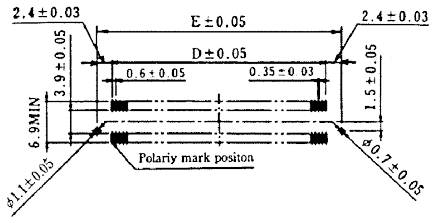
NOTE 1 : When ordering tube packaging, please do so in multiples of the tube packaging quantity.

NOTE 2 : Embossed tape packaging is available only for 60, 80, or 90-contact types. Connectors are sold by the reel with 1,000 pieces per reel. For details, see the section concerning the delivery form on Page 228 to 229.

◆ SINGLE UNIT RECOMMENDED PCB LAYOUT

Headers

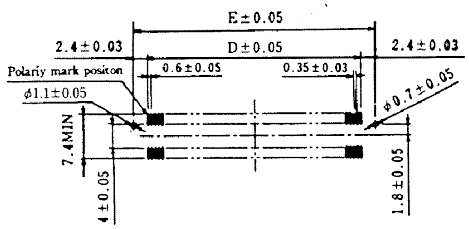
[FX8-※※P-SV]
[FX8-※※P-SV1]



※ Recommended metal mask thickness: t = 0.15 mm

Receptacles

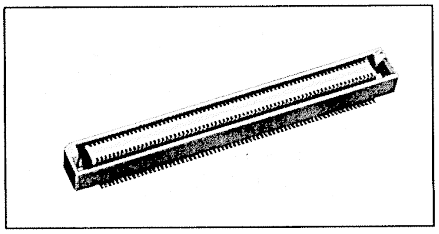
[FX8-※※S-SV]

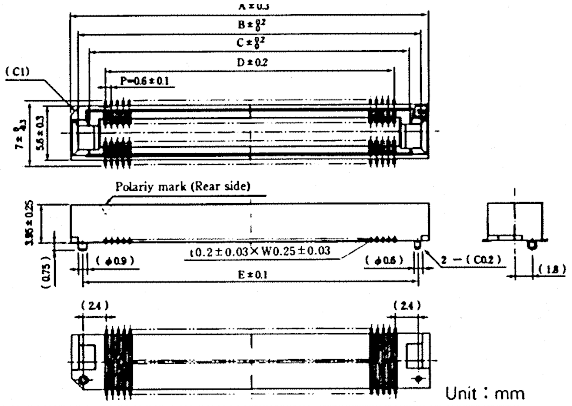


※ Recommended metal mask thickness: t = 0.15 mm
※ When the inside of the SMT pad (i.e., area beneath the connector mounting) has not been processed with insulating tape or some other material, that area is a pattern prohibited area.

FX8C-100S-SV5 Series Datasheet Excerpt

[FX8C-※※S-SV]



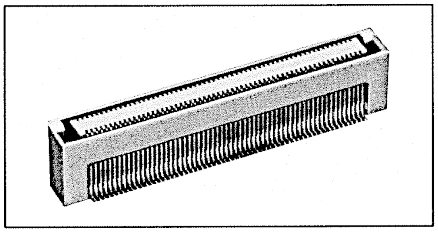


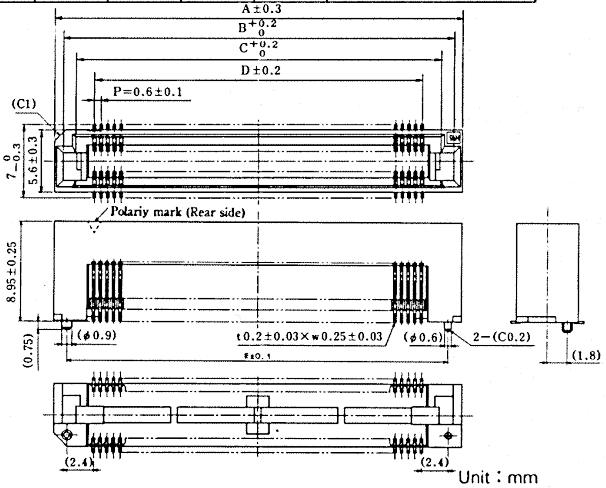
Unit : mm

HRS No.	Product No.	Number of Contacts	A	B	C	D	E	Magazine Packaging Volume (Pieces)
CL578-0801-2-※※	FX8C-60S-SV(※※)	60	24.60	23.05	20.80	17.40	22.20	21
CL578-0803-8-※※	FX8C-80S-SV(※※)	80	30.60	29.05	26.80	23.40	28.20	17
CL578-0805-3-※※	FX8C-100S-SV(※※)	100	36.60	35.05	32.80	29.40	34.20	14
CL578-0806-6-※※	FX8C-120S-SV(※※)	120	42.60	41.05	38.80	35.40	40.20	12
CL578-0807-9-※※	FX8C-140S-SV(※※)	140	48.60	47.05	44.80	41.40	46.20	10

※※ Blank : Tray packaged item 21 : Magazine packaged item
22 : Embossed tape packaged item
NOTE 1 : At the time of ordering magazine packaging, please order in multiples of the magazine packaging quantity.
NOTE 2 : Items available in embossed tape packaging are those with 60 or 80 contacts only. Also available in reel units. For details, see the sections dealing with delivery form on Pages 240 to 241.

[FX8C-※※S-SV5]





Unit : mm

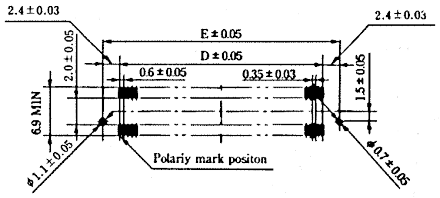
HRS No.	Product No.	Number of Contacts	A	B	C	D	E	Magazine Packaging Volume (Pieces)
CL578-0821-0-※※	FX8C-60S-SV5(※※)	60	24.60	23.05	20.80	17.40	22.20	21
CL578-0823-5-※※	FX8C-80S-SV5(※※)	80	30.60	29.05	26.80	23.40	28.20	17
CL578-0825-0-※※	FX8C-100S-SV5(※※)	100	36.60	35.05	32.80	29.40	34.20	14
CL578-0826-3-※※	FX8C-120S-SV5(※※)	120	42.60	41.05	38.80	35.40	40.20	12
CL578-0827-6-※※	FX8C-140S-SV5(※※)	140	48.60	47.05	44.80	41.40	46.20	10

※※ Blank : Tray packaged item 21 : Magazine packaged item 22 : Embossed tape packaged item
NOTE 1 : At the time of ordering magazine packaging, please order in multiples of the magazine packaging quantity.
NOTE 2 : Items available in embossed tape packaging are those with 60 or 80 contacts only. Also available in reel units. For details, see the sections dealing with delivery form on Pages 240 to 241.

◆ SINGLE UNIT RECOMMENDED PCB LAYOUT

Headers

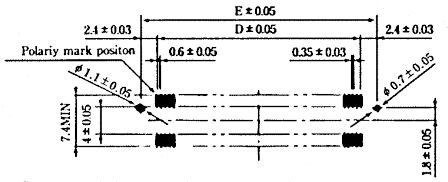
[FX8C-※※P-SV※]



※ Recommended metal mask thickness : t = 0.15mm

Receptacles

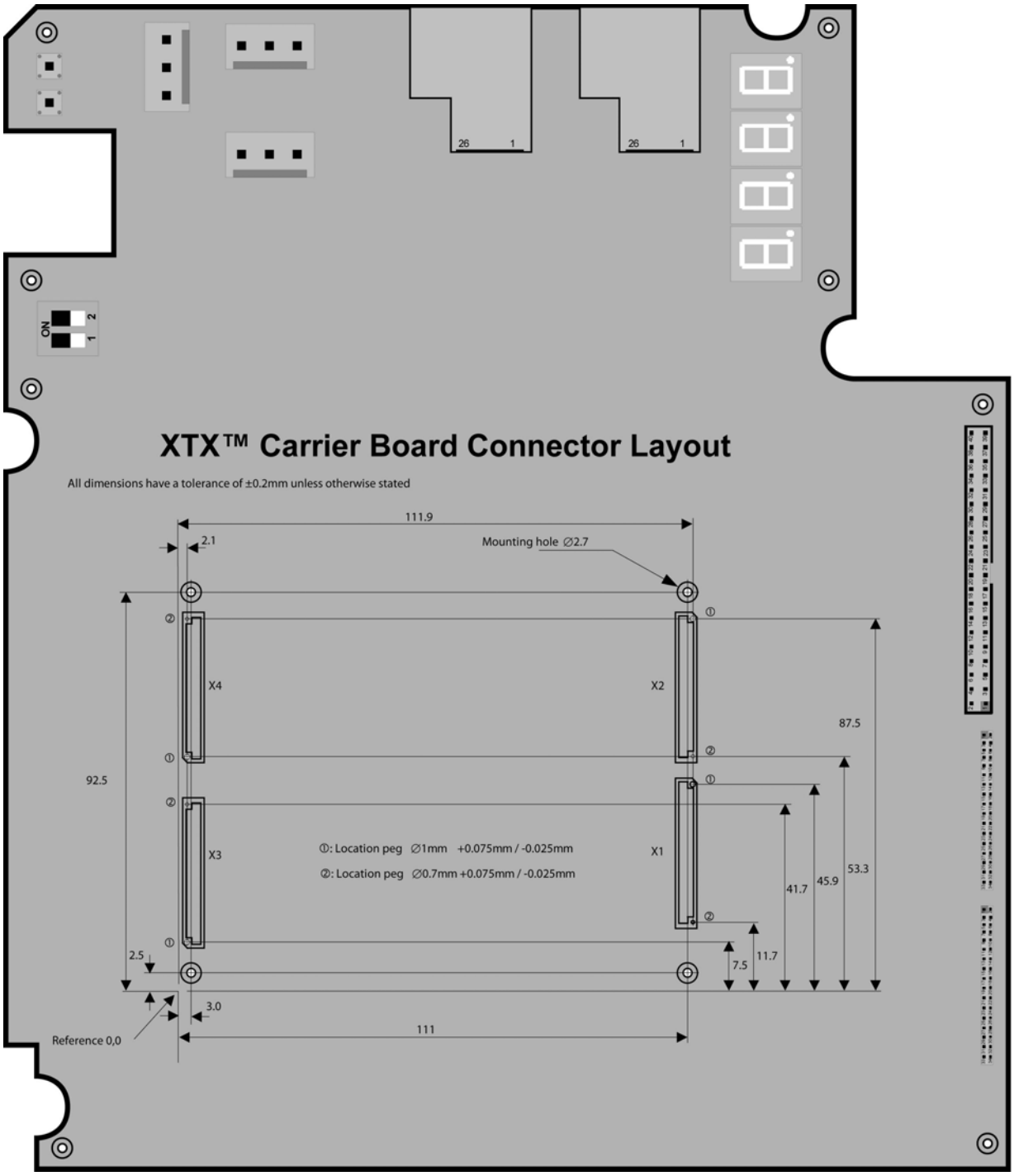
[FX8C-※※S-SV, SV5]



※ Recommended metal mask thickness : t=0.15mm
※ When the inside of the SMT pad (i.e., area beneath the connector mounting) has not been processed with insulating tape or some other material,that area is a pattern prohibited area.
(FX8C-※※S-SV5 is not applicable.)

1.4 Carrier Board Layout

The diagram below provides the dimensions for connector and mounting hole layout on an XTX™ Carrier Board. All dimensions have a tolerance of ±0.2mm unless otherwise stated.



2 Connector Pin Assignments

The following tables list the pin assignment for each of the four connectors located on the XTX™ module.

2.1 X1 Connector (PCI Bus, USB, Sound)

Table 1 X1 Connector Pinout

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	GND	2	GND	51	VCC	52	VCC
3	PCICLK3	4	PCICLK4	53	PAR	54	SERR#
5	GND	6	GND	55	GPERR#	56	Reserved
7	PCICLK1	8	PCICLK2	57	PME#	58	USB2#
9	REQ3#	10	GNT3#	59	LOCK#	60	DEVSEL#
11	GNT2#	12	3V	61	TRDY#	62	USB3#
13	REQ2#	14	GNT1#	63	IRDY#	64	STOP#
15	REQ1#	16	3V	65	FRAME#	66	USB2
17	GNT0#	18	RESERVED	67	GND	68	GND
19	VCC	20	VCC	69	AD16	70	CBE2#
21	SERIRQ	22	REQ0#	71	AD17	72	USB3
23	AD0	24	3V	73	AD19	74	AD18
25	AD1	26	AD2	75	AD20	76	USB0#
27	AD4	28	AD3	77	AD22	78	AD21
29	AD6	30	AD5	79	AD23	80	USB1#
31	CBE0#	32	AD7	81	AD24	82	CBE3#
33	AD8	34	AD9	83	VCC	84	VCC
35	GND	36	GND	85	AD25	86	AD26
37	AD10	38	AUXAL	87	AD28	88	USB0
39	AD11	40	MIC	89	AD27	90	AD29
41	AD12	42	AUXAR	91	AD30	92	USB1
43	AD13	44	ASVCC	93	PCIRST#	94	AD31
45	AD14	46	SNDL	95	INTC#	96	INTD#
47	AD15	48	ASGND	97	INTA#	98	INTB#
49	CBE1#	50	SNDR	99	GND	100	GND

2.2 X2 Connector (LPC Bus, SATA, PCI Express, ExpressCard, Audio Codec, additional USB)

Table 2 X2 Connector Pinout

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	GND	2	GND	51	VCC	52	VCC
3	PCIE_CLK_REF+	4	SATA0_RX+	53	PCIE1_RX-	54	SATA3_TX-
5	PCIE_CLK_REF-	6	SATA0_RX-	55	PCIE1_RX+	56	SATA3_TX+
7	GND	8	GND	57	GND	58	IL_SATA#
9	PCIE3_TX+	10	SATA0_TX-	59	PCIE1_TX-	60	PP_TPM
11	PCIE3_TX-	12	SATA0_TX+	61	PCIE1_TX+	62	RESERVED
13	GND	14	5V_SB	63	PCE_WAKE#	64	PCI_GNT#A
15	PCIE3_RX+	16	SATA1_RX+	65	SLP_S5#	66	PCI_REQ#A
17	PCIE3_RX-	18	SATA1_RX-	67	GND	68	GND
19	VCC	20	5V_SB	69	PCIE0_RX-	70	RESERVED
21	EXC1_CPPE#	22	SATA1_TX-	71	PCIE0_RX+	72	RESERVED
23	EXC1_RST#	24	SATA1_TX+	73	GND	74	VCC
25	USBP5	26	GND	75	PCIE0_TX-	76	RESERVED
27	USBP5#	28	SATA2_RX+	77	PCIE0_TX+	78	RESERVED
29	GND	30	SATA2_RX-	79	CODECSET	80	VCC
31	PCIE2_TX+	32	SUS_STAT#	81	AC_RST#	82	AC_SDOUT
33	PCIE2_TX-	34	PCI_CLKRUN#	83	VCC	84	VCC
35	GND	36	GND	85	AC_SYNC	86	AC_SDIN0
37	PCIE2_RX+	38	SATA2_TX-	87	AC_SDIN1	88	AC_SDIN2
39	PCIE2_RX-	40	SATA2_TX+	89	AC_BIT_CLK	90	FAN_TACHOIN
41	EXC0_CPPE#	42	GND	91	LPC_AD0	92	FAN_PWMOUT
43	EXC0_RST#	44	SATA3_RX+	93	LPC_AD1	94	LPC_FRAME#
45	USBP4	46	SATA3_RX-	95	LPC_AD2	96	LPC_DRQ0#
47	USBP4#	48	WDTRIG	97	LPC_AD3	98	LPC_DRQ1#
49	SLP_S3#	50	SATALED#	99	GND	100	GND

Caution

XTX™/ETX® compatibility

XTX™ modules can be operated on XTX™ compliant carrier boards as well as ETX® compliant carrier boards that do not use the ISA Bus. For the later case, please consult the XTX™ module's documentation on power consumption because the XTX™ specification defines additional VCC pins that are not present on ETX® compliant carrier board. The missing support for these pins on ETX® compliant carrier boards may result in exceeding the current rating for the XTX™ connectors.

XTX™ modules should not be operated on ETX® compliant carrier boards that use the ISA bus. Although the pinout of the new XTX™ connector is arranged in a way that avoids conflicts with the ISA bus pinout defined by the ETX® specification, the basic signaling levels of the ISA bus (5V) and the new interfaces defined by XTX™ (3.3V) are not compliant. Plugging a 3.3V compliant XTX™ module into an ETX® carrier board that uses 5V signaling on the ISA bus may result in damaging the hardware, presumably the XTX™ module.

2.3 X3 Connector (VGA, LCD, CRT, COM1, COM2, LPT/Floppy, IrDA, Mouse, Keyboard)

Table 3 X3 Connector Pinout

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	GND	2	GND	51	LPT/FLP#	52	RESERVED
3	R	4	B	53	VCC	54	GND
5	HSY	6	G	55	STB#/RESERVED	56	AFD#/DENSEL
7	VSY	8	DDCK	57	RESERVED	58	PD7/RESERVED
9	DETECT#	10	DDDA	59	IRRX	60	ERR#/HDSEL#
11	LCDDO16	12	LCDDO18	61	IRTX	62	PD6/RESERVED
13	LCDDO17	14	LCDDO19	63	RXD2	64	INIT#/DIR#
15	GND	16	GND	65	GND	66	GND
17	LCDDO13	18	LCDDO15	67	RTS2#	68	PD5/RESERVED
19	LCDDO12	20	LCDDO14	69	DTR2#	70	SLIN#/STEP#
21	GND	22	GND	71	DCD2#	72	PD4/DSKCHG#
23	LCDDO8	24	LCDDO11	73	DSR2#	74	PD3/RDATA#
25	LCDDO9	26	LCDDO10	75	CTS2#	76	PD2/WP#
27	GND	28	GND	77	TXD2	78	PD1/TRK0#
29	LCDDO4	30	LCDDO7	79	RI2#	80	PD0/INDEX#
31	LCDDO5	32	LCDDO6	81	VCC	82	VCC
33	GND	34	GND	83	RXD1	84	ACK#/DRV
35	LCDDO1	36	LCDDO3	85	RTS1#	86	BUSY/MOT
37	LCDDO0	38	LCDDO2	87	DTR1#	88	PE/WDATA#
39	VCC	40	VCC	89	DCD1#	90	SLCT/WGATE#
41	FPDDC_DAT	42	LTGIO0	91	DSR1#	92	MSCLK
43	FPDDC_CLK	44	BLON#	93	CTS1#	94	MSDAT
45	BIASON	46	DIGON	95	TXD1	96	KBCLK
47	COMP	48	Y	97	RI1#	98	KBDAT
49	SYNC	50	C	99	GND	100	GND

Note

The above table includes the pinout for both LPT and Floppy modes. If a column has

two signal names listed, for example AFD#/DENSEL, then the first refers to when the module is in LPT mode and the second refers to when in Floppy mode.

2.4 X4 Connector (IDE 1, IDE 2, Ethernet, Miscellaneous)

Table 4 X4 Connector Pinout

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	GND	2	GND	51	SIDE_IOW#	52	PIDE_IOR#
3	5V_SB	4	PWGIN	53	SIDE_DRQ	54	PIDE_IOW#
5	PS_ON#	6	SPEAKER	55	SIDE_D15	56	PIDE_DRQ
7	PWRBTN#	8	BATT	57	SIDE_D0	58	PIDE_D15
9	KBINH#	10	LILED#	59	SIDE_D14	60	PIDE_D0
11	RSMRST#	12	ACTLED#	61	SIDE_D1	62	PIDE_D14
13	ROMKBCS#	14	SPEEDLED#	63	SIDE_D13	64	PIDE_D1
15	EXT_PRG	16	I2CLK	65	GND	66	GND
17	VCC	18	VCC	67	SIDE_D2	68	PIDE_D13
19	OVCR#	20	GPCS#	69	SIDE_D12	70	PIDE_D2
21	EXTSMI#	22	I2DAT	71	SIDE_D3	72	PIDE_D12
23	SMBCLK	24	SMBDATA	73	SIDE_D11	74	PIDE_D3
25	SIDE_CS3#	26	SMBALRT#	75	SIDE_D4	76	PIDE_D11
27	SIDE_CS1#	28	DASP_S	77	SIDE_D10	78	PIDE_D4
29	SIDE_A2	30	PIDE_CS3#	79	SIDE_D5	80	PIDE_D10
31	SIDE_A0	32	PIDE_CS1#	81	VCC	82	VCC
33	GND	34	GND	83	SIDE_D9	84	PIDE_D5
35	PDIAG_S	36	PIDE_A2	85	SIDE_D6	86	PIDE_D9
37	SIDE_A1	38	PIDE_A0	87	SIDE_D8	88	PIDE_D6
39	SIDE_INTRQ	40	PIDE_A1	89	GPE2#	90	CBLID_P#
41	BATLOW#	42	GPE1#	91	RXD#	92	PIDE_D8
43	SIDE_AK#	44	PIDE_INTRQ	93	RXD	94	SIDE_D7
45	SIDE_RDY	46	PIDE_AK#	95	TXD#	96	PIDE_D7
47	SIDE_IOR#	48	PIDE_RDY	97	TXD	98	HDRST#
49	VCC	50	VCC	99	GND	100	GND

3 Signal Descriptions

The "#" symbol at the end of the signal name indicates that the active, or asserted state, occurs when the signal is at a low voltage level. When "#" is not present, the signal is asserted when at a high voltage level.

The following terminology is used to describe the signals types in the I/O columns for the tables located below.

Term	Description
I	Input Pin
O	Output Pin
OC	Open Collector Output Pin
I/O	Bi-directional Input/Output Pin
P	Power Input/Output

3.1 X1 Connector Signal Descriptions

Table 5 Signal Descriptions

Signal	Description	I/O
VCC	Power Supply +5VDC ±5%	P
GND	Power Ground	P
3V	+3.3V ± 5% supply voltage generated onboard the XTX module. These two pins may be used as a power supply for external devices. Maximum allowable external load is 500mA.	P
RESERVED	Do not connect.	
SERIRQ	Serial interrupt request. This pin is used to support the serial interrupt protocol.	I

Table 6 PCI Signal Descriptions

Signal	Description of PCI Bus Signals	I/O
PCICLK1..4.	PCI clock outputs for external PCI devices.	O
REQ0..3#	Bus Request signals of PCI Masters. When asserted, it means the PCI Master is requesting the PCI bus ownership from the arbiter.	I
GNT0..3#	Grant signals to PCI Masters. When asserted by the arbiter, it means the PCI master has been legally granted to own the PCI bus.	O
AD0..31	PCI Address and Data Bus Lines. These lines are connected to the PCI bus. AD[31:0] contain the information of address or data for PCI transactions.	I/O
CBE0..3#	PCI Bus Command and Byte Enables. Bus commands and byte enables are multiplexed in these lines for address and data phases, respectively.	I/O
PAR	Parity bit of PCI bus. It is the even parity bit across PAD[31:0] and CBE#[3:0].	I/O
SERR#	System Error or PCI Clock RUN. If the Northbridge detects parity errors in DRAMs, it will assert SERR# to notify the system.	I/O
GPERR#	Parity Error. For PCI operation per exception granted by PCI 2.1 specification.	I/O
PME#	Power management event.	I/O
LOCK#	Lock Resource Signal. This pin indicates the PCI master or the bridge intends to do exclusive transfers.	I/O
DEVSEL#	Device Select. When the target device has decoded the address as its own cycle, it will assert DEVSEL#.	I/O
TRDY#	Target Ready. This pin indicates the target is ready to complete the current data phase of transaction.	I/O
IRDY#	Initiator Ready. This signal indicates the initiator is ready to complete the current data phase of transaction.	I/O
STOP#	Stop. This signal indicates the target is requesting the master to stop the current transaction.	I/O
FRAME#	Cycle Frame of PCI Buses. This indicates the beginning and duration of a PCI access. It will be as an output driven by Northbridge on behalf of CPU, or as an input during PCI master access.	I/O
PCIRST#	PCI Bus Reset. This is an output signal to reset the entire PCI Bus. This signal will be asserted during system reset and is a logic invert of RSTDRV.	O
INTA#	PCI interrupt pin A	I
INTB#	PCI interrupt pin B	I
INTC#	PCI interrupt pin C	I
INTD#	PCI interrupt pin D	I

Table 7 USB Signal Descriptions

Signal	Description of USB Signals	I/O
USB0	USB Port 0, data + or D+	I/O
USB0#	USB Port 0, data - or D-	I/O
USB1	USB Port 1, data + or D+	I/O
USB1#	USB Port 1, data - or D-	I/O
USB2	USB Port 2, data + or D+	I/O
USB2#	USB Port 2, data - or D-	I/O
USB3	USB Port 3, data + or D+	I/O
USB3#	USB Port 3, data - or D-	I/O

Table 8 Audio Signal Descriptions

Signal	Description of Audio Signals	I/O
SNDL	Line-level stereo output left. This pin can drive a 5k Ohm AC load.	O
SNDR	Line-level stereo output right. This pin can drive a 5k Ohm AC load.	O
AUXAL	Auxiliary A input left. Normally intended for connection to an internal or external CD-ROM analog output.	I
AUXAR	Auxiliary A input right. Normally intended for connection to an internal or external CD-ROM analog output.	I
MIC	Microphone input.	I
ASGND	Analog ground for sound controller.	P
ASVCC	Analog supply voltage for sound controller.	P

3.2 X2 Connector Signal Descriptions

Table 9 Signal Descriptions

Signal	Description	I/O
VCC	Power Supply +5VDC, ±5%	P
GND	Power Ground	P
RESERVED	Do not connect.	

Table 10 LPC Interface Signal Descriptions

Signal	Description	I/O
LPC_AD[0..3]	Multiplexed Command, Address and Data.	I/O
LPC_FRAME#	Frame: Indicates start of a new cycle or termination of a broken cycle.	O
LPC_DRQ[0..1]#	Encoded DMA/Bus Master Request.	I

Table 11 Serial ATA Signal Descriptions

Signal	Description	I/O
SATA0_RX+ SATA0_RX-	Serial ATA channel 0, Receive Input differential pair.	I
SATA0_TX+ SATA0_TX-	Serial ATA channel 0, Transmit Output differential pair.	O
SATA1_RX+ SATA1_RX-	Serial ATA channel 1, Receive Input differential pair.	I
SATA1_TX+ SATA1_TX-	Serial ATA channel 1, Transmit Output differential pair.	O
SATA2_RX+ SATA2_RX-	Serial ATA channel 2, Receive Input differential pair.	I
SATA2_TX+ SATA2_TX-	Serial ATA channel 2, Transmit Output differential pair.	O
SATA3_RX+ SATA3_RX-	Serial ATA channel 3, Receive Input differential pair.	I
SATA3_TX+ SATA3_TX-	Serial ATA channel 3, Transmit Output differential pair.	O
IL_SATA#	Serial ATA Interlock Switch Input.	I
SATALED#	Serial ATA Led. Open collector output pin driven during SATA command activity.	OC

Table 12 PCI Express Signal Descriptions

Signal	Description	I/O
PCIE0_RX+ PCIE0_RX-	PCI Express channel 0, Receive Input differential pair.	I
PCIE0_TX+ PCIE0_TX-	PCI Express channel 0, Transmit Output differential pair.	O
PCIE1_RX+ PCIE1_RX-	PCI Express channel 1, Receive Input differential pair.	I
PCIE1_TX+ PCIE1_TX-	PCI Express channel 1, Transmit Output differential pair.	O
PCIE2_RX+ PCIE2_RX-	PCI Express channel 2, Receive Input differential pair.	I
PCIE2_TX+ PCIE2_TX-	PCI Express channel 2, Transmit Output differential pair.	O
PCIE3_RX+ PCIE3_RX-	PCI Express channel 3, Receive Input differential pair.	I
PCIE3_TX+ PCIE3_TX-	PCI Express channel 3, Transmit Output differential pair.	O
PCIE_CLK_REF+ PCIE_CLK_REF-	PCI Express Reference Clock for Lanes 0 to 3.	O
PCE_WAKE#	PCI Express Wake Event: Sideband wake signal asserted by components requesting wakeup.	I

Note

There is a total of 4 PCIe TX and RX differential pairs supported on the XTX™ connector. Depending on the features supported by the XTX™ module and the core logic chipset used, these lines may be used to form x1, x2 or x4 PCI Express links. The documentation for the XTX™ module shall clearly identify which PCI Express link configuration or configurations (in the case that these can be programmed in the core logic chipset) are supported.

Table 13 ExpressCard Support Pins Descriptions

Signal	Description	I/O
EXEC_CPPE[0..1]#	ExpressCard capable card request.	I
EXEC_RST[0..1]#	ExpressCard Reset	O

Table 14 Audio Codec Signal Descriptions

Signal	Description	I/O
AC_RST#	CODEC Reset	O
AC_SYNC	Serial Bus Synchronization.	O
AC_BIT_CLK	12.228 MHz Serial Bit Clock from CODEC.	O
AC_SDOUT	Audio Serial Data Output to CODEC.	O
AC_SDIN[0..2]	Audio Serial Data Input from CODEC0..CODEC2.	I
CODECSET	Disable onboard Audio Codec.	I

Table 15 USB Signal Descriptions

Signal	Description	I/O
USBP4	Universal Serial Bus Port 4 positive differential signal.	I/O
USBP4#	Universal Serial Bus Port 4 negative differential signal.	I/O
USBP5	Universal Serial Bus Port 5 positive differential signal.	I/O
USBP5#	Universal Serial Bus Port 5 negative differential signal.	I/O

Table 16 Miscellaneous Signal Descriptions

Signal	Description	I/O
GND	Ground. All GND pins should be connected to the carrier board ground plane.	-
5V_SB	Additional Power input for the internal suspend and power-control circuitry. This Signal is connected to ETX®-Connector X4/Pin3. Refer to ETX® Specification for further details.	I
VCC	5V Power Input. All VCC pins should be connected to the carrier board 5 Volt power plane.	I
SUS_STAT#	Suspend Status: indicates that the system will be entering a low power state soon.	O
SLP_S3#	S3 Sleep Control: This signal shuts off power to all non-critical systems when in S3 (Suspend to Ram), S4 or S5 states.	O
SLP_S5#	S5 Sleep Control: This signal shuts off power to all non-critical systems when in S5 (Soft Off) state.	O
PCI_CLKRUN#	PCI Clock Run: This signal is used to support PCI Clock Run protocol. It connects to PCI devices that need to request clock re-start, or prevention of clock stopping.	I/O
PCI_GNT#A	reserved	O
PCI_REQ#A	reserved	I
FAN_PWMOUT	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the Fan's RPM.	OC
FAN_TACHOIN	Fan tachometer input.	I
WDTRIG	Watch Dog Trigger Signal.	I
PP_TPM	Physical Presence pin of Trusted Platform Module (TPM). Active high. TPM chip has an internal pull-down. This signal is used to indicate Physical Presence to the TPM.	I

3.3 X3 Connector Signal Descriptions

Table 17 Signal Descriptions

Signal	Description	I/O
VCC	Power Supply +5VDC, ±5%	P
GND	Power Ground	P
RESERVED	Do not connect.	
LTGIO0	General purpose I/O	I/O

Table 18 CRT Signal Descriptions

Signal	Description of CRT signals	I/O
HSY	Horizontal Sync: This output supplies the horizontal synchronization pulse to the monitor. It is normally not needed for flat panels.	O
VSY	Vertical Sync: This output supplies the vertical synchronization pulse to the monitor. It is normally not needed for flat panels.	O
R	CRT analog video output.	O
G	CRT analog video output.	O
B	CRT analog video output.	O
DDCK	Display Data Channel Clock. This pin is functionally suitable for a DDC interface between the graphics controller chip and the CRT monitor.	I/O
DDDA	Display Data Channel Data. This pin is functionally suitable for a DDC interface between the graphics controller chip and the CRT monitor.	I/O

Table 19 TV Signal Descriptions

Signal	Description of CRT signals	I/O
SYNC	Composite Sync for SCART PAL TV's that use the EURO AV Connector. It is fed to the "Video In" pin of this connector to provide a signal that the TV can overlay the RGB data onto. This pin may also be used as a general I/O pin for controlling video switch, or for the other internal timing signals including Hsync, Vsync, etc.	I/O
Y	Luminance for S-Video or Red for RGB Video.	O
C	Chrominance for S-Video or Green for RGB Video.	O
COMP	Composite Video or Blue for RGB Video.	O

Table 20 LCD Flat Panel Signals

Signal	Description of LCD Flat Panel signals	I/O
BIASON	Controls display contrast voltage ON	O
DIGON	Controls display Power ON	O
BLON#	Controls display Backlight ON	O
LCDDO0..19	LVDS channel data 0..19	O
DETECT#	Panel hot-plug detection	I
FPDDC_CLK	DDC lines used for flat panel detection and control.	O
FPDDC_DAT	DDC lines used for flat panel detection and control.	I/O

Table 21 COM Signal Descriptions

Signal	Description of COM signals	I/O
DTR1#	Active low data terminal ready output for the serial port. Handshake output signal notifies modem that the UART is ready to establish data communication link.	O
DTR2#	Active low data terminal ready output for the serial port. Handshake output signal notifies modem that the UART is ready to establish data communication link.	O
RI1#, RI2#	This active low input is for the serial port. Handshake signal which notifies the UART that the telephone ring signal is detected by the modem.	I
TXD1, TXD2	Transmitter serial data output from Serial port.	O
RXD1, RXD2	Receiver serial data input.	I
CTS1#, CTS2#	These active low inputs are for serial ports . Handshake signal, which notifies the UART that the modem is ready to receive data.	I
RTS1#, RTS2#	These active low inputs are for serial ports. Handshake signal notifies the modem that the UART is ready to transmit data.	O
DCD1#, DCD2#	These active low inputs are for serial ports. Handshake signal, which notifies the UART that carrier signal is detected by the modem.	I
DSR1#, DSR2#	These active low inputs are for serial ports. Handshake signal which notifies the UART that the modem is ready to establish the communication link.	I

Table 22 Keyboard and Infrared Signal Descriptions

Signal	Description of keyboard and infrared signals	I/O
KBDAT	This is the bidirectional keyboard data signal.	I/O
KBCLK	This is the keyboard clock signal.	O
MSDAT	This is the bidirectional mouse data signal.	I/O
MSCLK	This is the mouse clock signal.	O
IRTX	Infrared transmit pin.	O
IRRX	Infrared receive pin.	I

The LPT and FDC (Floppy Drive Controller) share the same pins on the X3 connector. Only one interface is available at any given time. Table 23 describes the signals when in LPT mode and table 24 describes the signals when in Floppy mode.

Table 23 LPT Signal Descriptions

Signal	Description of LPT signals (shared with FDC)	I/O
LPT	LPT Interface configuration input	I
STB#	This active low pulse is used to strobe the printer data into the printer.	O
AFD#	This active low output causes the printer to automatically feed one line after each line is printed.	O
PD0.....7	This bidirectional parallel data bus is used to transfer information between CPU and peripherals.	I/O
ERR#	This active low signal indicates an error situation at the printer.	I
INIT#	This active low signal is used to initiate the printer when low.	O
SLIN#	This active low signal selects the printer.	O
ACK#	This active low output from the printer indicates it has received the data and is ready to receive new data.	I
BUSY	This signal indicates the printer is busy and not ready to receive new data.	I
PE	This signal indicates that the printer is out of paper.	I
SLCT	This active high output from the printer indicates that it has power on.	I

Table 24 FDC Signal Descriptions

Signal	Description of FDC signals (shared with LPT)	I/O
FLPY#	Floppy Interface configuration input	I
RES	Do not connect	N.A.
DENSEL	Indicates whether a low (250/300Kb/s) or high (500/1000Kbs) data rate has been selected.	O
INDEX#	This active low Schmitt Trigger input signal senses from the disk drive that the head is positioned over the beginning of a track, as marked by an index hole.	I
TRK0#	This active low Schmitt Trigger input signal senses from the disk drive that the head is positioned over the outermost track.	I
WP#	This active-low Schmitt Trigger input signal senses from the disk drive that a disk is write-protected.	I
RDATA#	The active-low, raw data read signal from the disk is connected here. Each falling edge represents a flux transition of the encoded data.	I
DSKCHG#	This disk interface input indicates when the disk drive door has been opened. This active-low signal is read from bit D7 of location base+7.	I
HDSEL#	This active low output determines which disk drive head is active. Low = Head 0, high (open) = Head 1.	O
DIR#	This active low output determines the direction of the head movement (low = step-in, high = step-out).	O
STEP#	This active low output signal produces a pulse at a software-programmable rate to move the head during a seek operation.	O
DRV	This signal selects the floppy drive.	O
MOT#	This active-low output activates the disk drive motor.	O
WDATA#	This active low output is a write-precompensated serial data stream to be written onto the selected disk drive. Each falling edge causes a flux change on the media.	O
WGATE#	This active-low, high-drive output enables the write circuitry of the selected disk drive.	O

3.4 X4 Connector Signal Descriptions

Table 25 Signal Descriptions

Signal	Description	I/O
VCC	Power Supply +5VDC, ±5%	P
GND	Power Ground	P

Table 26 IDE Signal Descriptions

Signal	Description of IDE signals	I/O
PIDE_D0..15	Primary IDE ATA Data Bus. These are the Data pins connected to Primary Channel.	I/O
PIDE_A0..2	Primary IDE ATA Address Bus. These are the Address pins connected to Primary Channel.	O
PIDE_CS1#	IDE Chip Select 1 for Primary Channel 0. This is the Chip Select 1 command output pin to enable the Primary IDE device to watch the Read/Write Command.	O
PIDE_CS3#	IDE Chip Select 3 for Primary Channel 1. This is the Chip Select 3 command output pin to enable the Primary IDE device to watch the Read/Write Command.	O
PIDE_DRQ	Primary IDE DMA Request for IDE Master. This is the input pin from the Primary Channel IDE DMA request to do the IDE Master Transfer. It will active high in DMA or Ultra-33 mode and always be inactive low in PIO mode.	I
PIDED_AK#	Primary IDE DACK# for IDE Master. This is the output pin to grant the Primary Channel IDE DMA request to begin the IDE Master Transfer in DMA or Ultra-33 mode.	O
PIDE_RDY	Primary IDE Ready. This is the input pin from the Primary IDE Channel to indicate the IDE device is ready to terminate the IDE command in PIO mode. The IDE device can deassert this input (logic 0) to expand the IDE command if the device is not ready. In Ultra-33 mode, this pin has different functions. In read cycles, IDE device will drive this signal as Data Strobe (DSTROBE) to be used by IDE Busmaster to strobe the input data. In write cycle, this pin is used by IDE device to notify IDE Busmaster as DMA Ready (DDMARDY#).	I
PIDE_IOR#	Primary IDE IOR# Command. This is the IOR# command output pin to notify the Primary IDE device to assert the Read Data in PIO and DMA mode. In Ultra-33 mode, this pin has different functions. In read cycle, this pin is used by IDE Busmaster to notify IDE device as DMA Ready (DDMARDY#). In write cycle, IDE Busmaster will drive this signal as Data Strobe (DSTROBE) to use by IDE device to strobe the output data.	O
PIDE_IOW#	Primary IDE IOW# Command. This is the IOW# command output pin to notify the Primary IDE device that the available Write Data is already asserted by IDE Busmaster in PIO and DMA mode. In Ultra-33 mode, this pin is driven by IDE Busmaster to force IDE device to terminate current transaction. After receiving this input, IDE device will deassert DRQ to STOP current transaction.	O
PIDE_INTRQ	Primary channel interrupt signal.	I
SIDE_D0..15	Secondary IDE ATA Data Bus. These are the Data pins connected to Secondary Channel.	I/O
SIDE_A0..2	Secondary IDE ATA Address Bus. These are the Address pins connected to Secondary Channel.	O
SIDE_CS1#	IDE Chip Select 1 for Secondary Channel 0. This is the Chip Select 1 command output pin to enable the Secondary IDE device to watch the Read/Write Command.	O
SIDE_CS3#	IDE Chip Select 3 for Secondary Channel 1. This is the Chip Select 3 command output pin to enable the Secondary IDE device to watch the Read/Write Command.	O
SIDE_DRQ	Secondary IDE DMA Request for IDE Master. This is the input pin from the Secondary Channel IDE DMA request to do the IDE Master Transfer. It will active high in DMA or Ultra-33 mode and always be inactive low in PIO mode.	I

SIDED_AK#	Secondary IDE DACK# for IDE Master. This is the output pin to grant the Secondary Channel IDE DMA request to begin the IDE Master Transfer in DMA or Ultra-33 mode.	O
SIDE_RDY	Secondary IDE Ready. This is the input pin from the Secondary IDE Channel to indicate the IDE device is ready to terminate the IDE command in PIO mode. The IDE device can deassert this input (logic 0) to expand the IDE command if the device is not ready. In Ultra-33 mode, this pin has different functions. In read cycle, IDE device will drive this signal as Data Strobe (DSTROBE) to use by IDE Busmaster to strobe the input data. In write cycles, this pin is used by IDE device to notify IDE Busmaster as DMA Ready (DDMARDY#).	I
SIDE_IOR#	Secondary IDE IOR# Command. This is the IOR# command output pin to notify the Secondary IDE device to assert the Read Data in PIO and DMA mode. In Ultra-33 mode, this pin has different function. In read cycle, this pin is used by IDE Busmaster to notify IDE device as DMA Ready (DDMARDY#). In write cycle, IDE Busmaster will drive this signal as Data Strobe (DSTROBE) to use by IDE device to strobe the output data.	O
SIDE_IOW#	Secondary IDE IOW# Command. This is the IOW# command output pin to notify the Secondary IDE device that the available Write Data is already asserted by IDE Busmaster in PIO and DMA mode. In Ultra-33 mode, this pin is driven by IDE Busmaster to force IDE device to terminate current transaction. After receiving this input, IDE device will deassert DRQ to STOP current transaction.	O
SIDE_INTRQ	Secondary channel interrupt signal.	I
DASP_S	Time-multiplexed, open collector output which indicates that a drive is active, or that a slave drive is present on Secondary IDE channel. Necessary for using IDE master/slave-mode on Secondary IDE channel.	O
PDIAG_S	Output by the drive if it is jumpered in the slave mode; input to the drive if it is jumpered in the master mode. The signal indicates to a master that the slave has passed its internal Diagnostic command. Necessary for using IDE master/slave-mode on Secondary IDE channel.	I
HDRST#	Low active hardware reset (RSTDRV inverted).	O
CBLID_P#	This pin may be used to detect the presence of an 80-conductor IDE cable on the primary IDE channel. This allows BIOS or system software to determine whether to enable high-speed transfer modes.	I

Table 27 Ethernet Signal Descriptions

Signal	Description of Ethernet signals	I/O
TXD#, TXD	Analog Twisted Pair Ethernet Transmit Differential Pair. These pins transmit the serial bit stream for transmission on the Unshielded Twisted Pair (UTP) cable. The current-driven differential driver can be two-level (10BASE-T) or three-level (100BASE-TX) signals depending on the mode of operation. These signals interface directly with an isolation transformer.	O
RXD#, RXD	Analog Twisted Pair Ethernet Receive Differential Pair. These pins receive the serial bit stream from the isolation transformer. The bit stream can be two-level (10BASE-T) or three-level (100BASE- TX) signals depending on the mode of operation.	I
ACTLED#	The Activity LED pin indicates either transmit or receive activity. When activity is present, the activity LED is on; when no activity is present, the activity LED is off.	O
LILED#	The Link Integrity LED pin indicates link integrity. If the link is valid in either 10 or 100 Mbps, the LED is on; if link is invalid, the LED is off.	O
SPEEDLED#	The Speed LED pin indicates the speed. The speed LED will be on at 100 Mbps and off at 10 Mbps.	O

Table 28 Power Control Signals

Signal	Description of Power Control signals	I/O
PWGIN	High active input for the XTX-PC indicates that power from the power supply is ready. It can also be used as low active reset input signal.	I
5V_SB	Power supply pin for internal Suspend circuit. AT or ATX hardware configure input.	P
PS_ON#	Remove All Circuit Power Except Internal Suspend Circuit. PS_ON will become active high to disable all the circuits except internal Suspend circuit.	O
PWRBTN#	Power Button Input. This input is used to support the ACPI Power Button function.	I

Table 29 Power Management Signals

Signal	Description of Power Management signals	I/O
RSMRST#	Resume Reset input. This input may be driven low by external circuitry to reset the power management logic on the XTX module.	I
SMBALRT#	System Management Bus Alert input. This signal may be driven low by SMB devices to signal an event on the SM Bus.	I
BATLOW#	Battery low input. This signal may be driven low by external circuitry to signal that the system battery is low, or may be used to signal some other external power-management event.	I
GPE1#	General-purpose, power-management event input 1. This may be driven low by external circuitry to signal an external power-management event.	I
GPE2#	General-purpose, power-management event input 2. This may be driven low by external circuitry to signal an external power-management event.	I
EXTSMI#	System-management-interrupt input. This may be driven low by external circuitry to initiate an SMI.	I

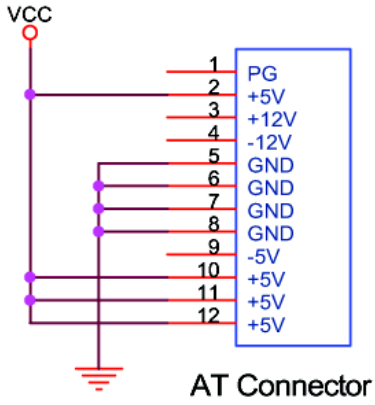
Table 30 Miscellaneous Signal Descriptions

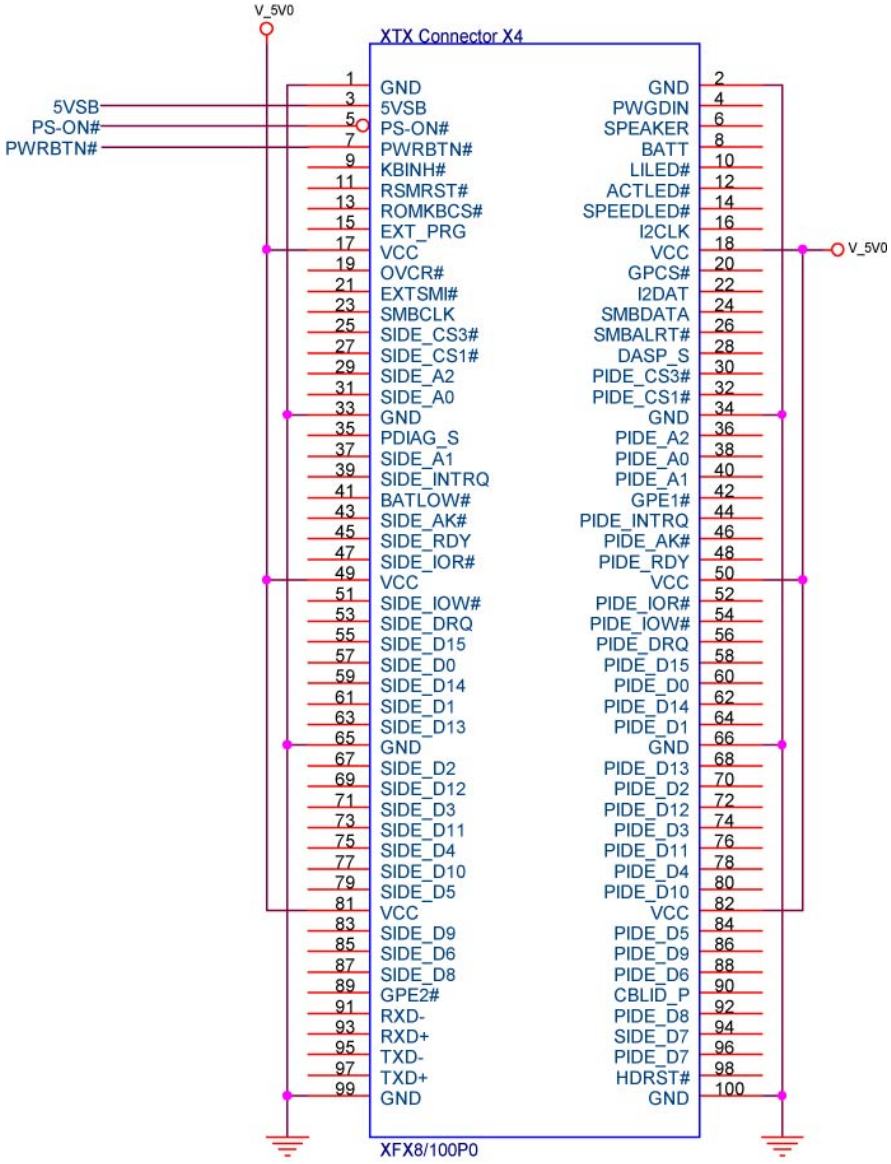
Signal	Description of Miscellaneous signals	I/O
SPEAKER	This is the speaker output signal, connected to a speaker between output and VCC.	O
BATT	3 V backup cell input. BATT should be connected to a 3V backup cell for RTC operation and storage register non-volatility in the absence of system power. (VBATT = 2.4 - 3.3 V)	I
I^2CLK	Clock line of I2C-Bus.	I/O
I^2DAT	Data line of I2C-Bus.	I/O
SMBCLK	Clock line of SM-Bus.	I/O
SMBDATA	Data line of SM-Bus.	I/O
KBINH#	Keyboard Inhibit.	I
OVCR#	Over current detect input. This pin is used to monitor the USB power over current.	I
ROMKBCS#	For internal use only. Do not connect.	
EXT_PRG	For internal use only. Do not connect.	
GPCS#	For internal use only. Do not connect.	

3.4.1 AT Power Requirements

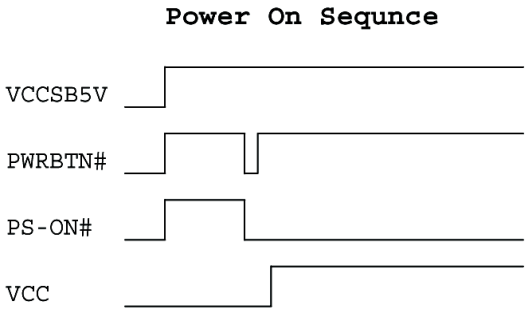
Note

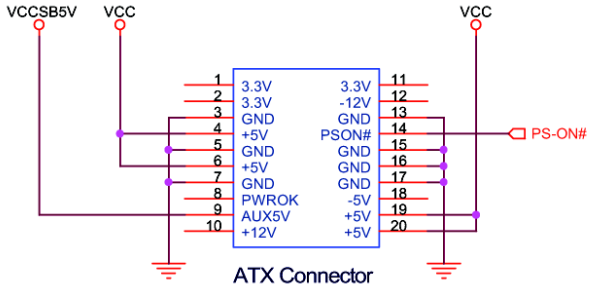
If an AT power supply is to be used then the 5V_SB, PS_ON#, and PWRBTN# pins should be left unconnected.

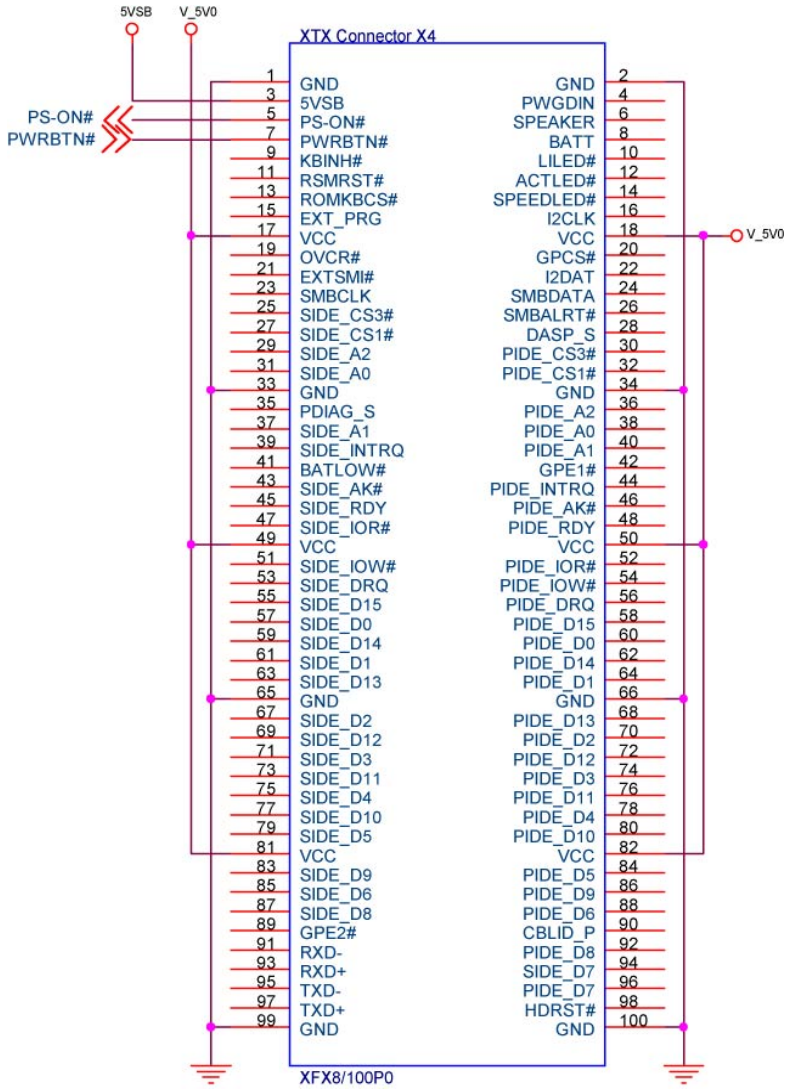




3.4.2 ATX Power Requirements

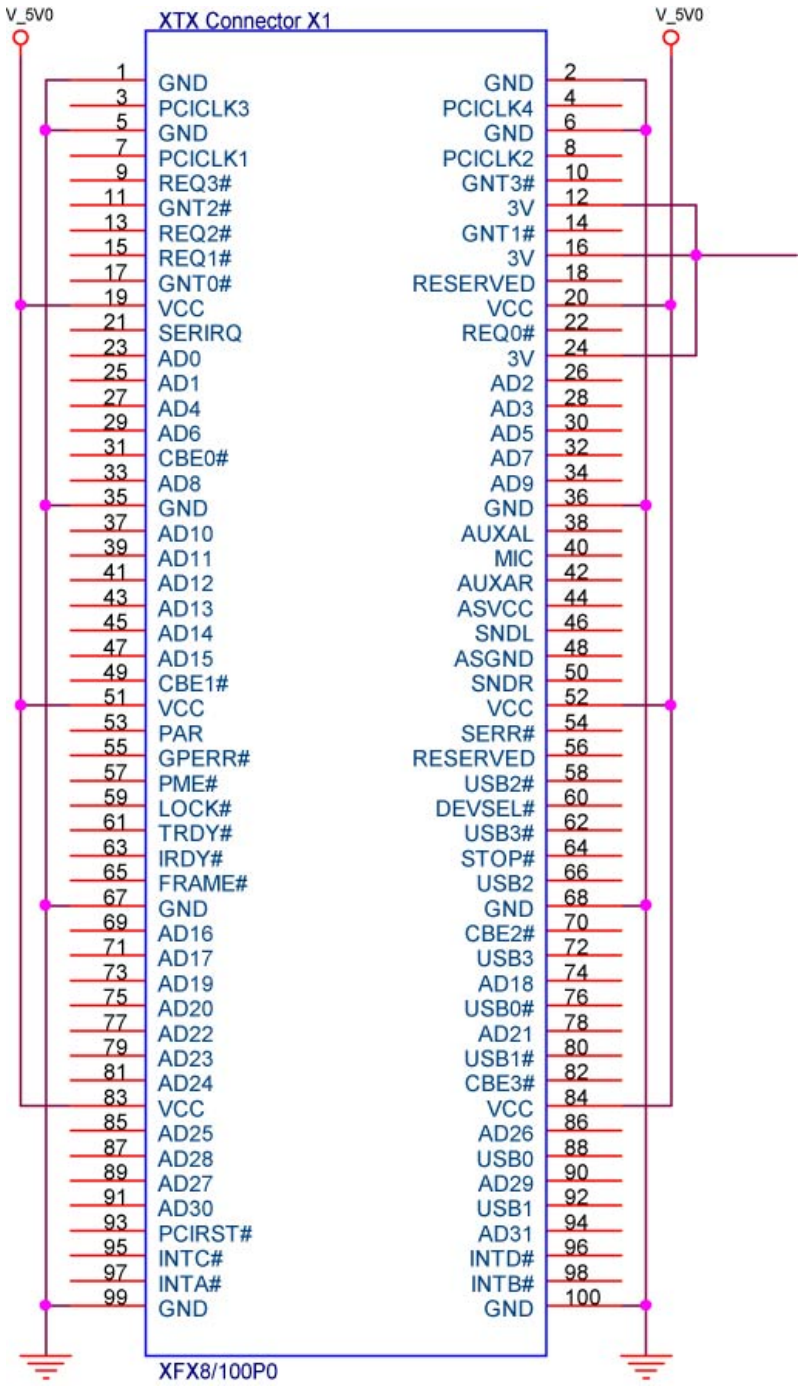




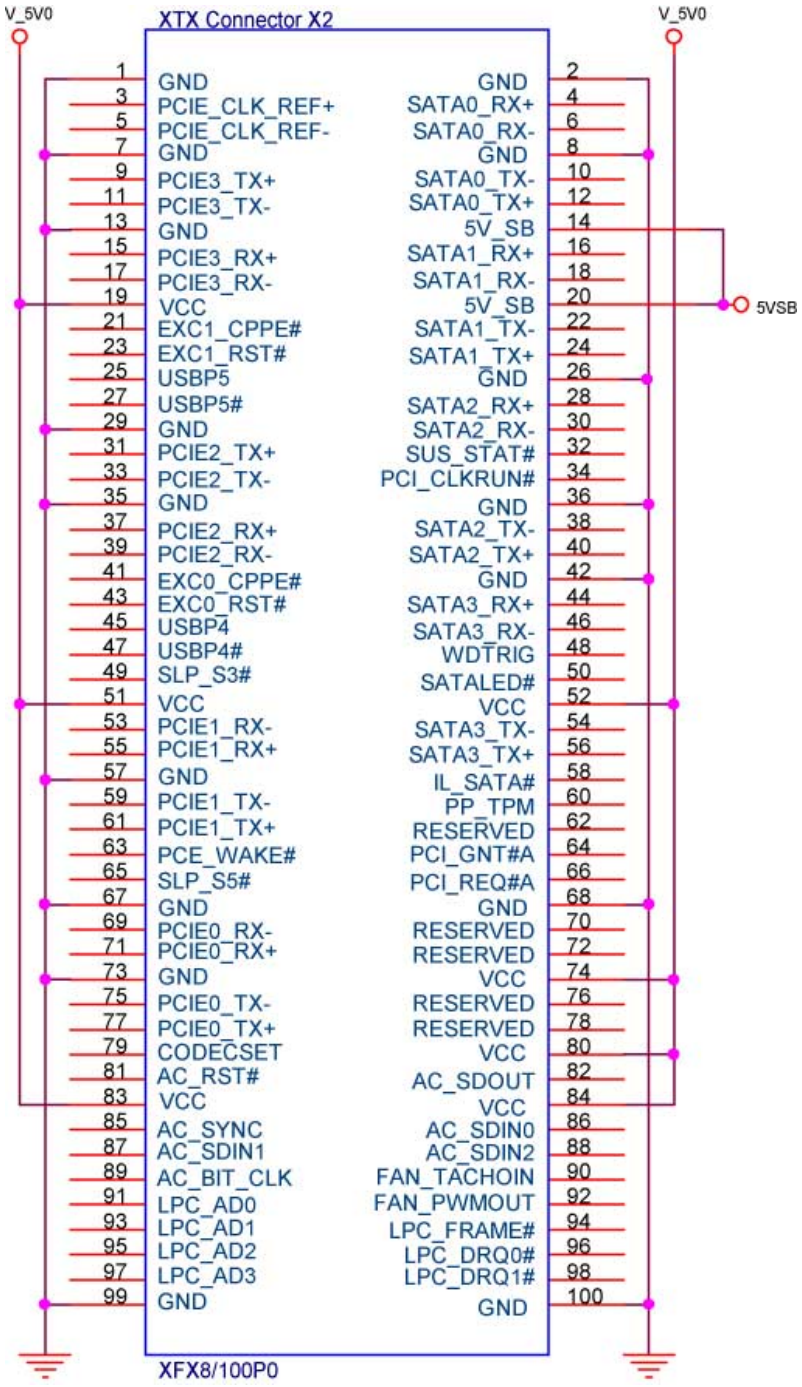


4 Connector Schematics Symbol

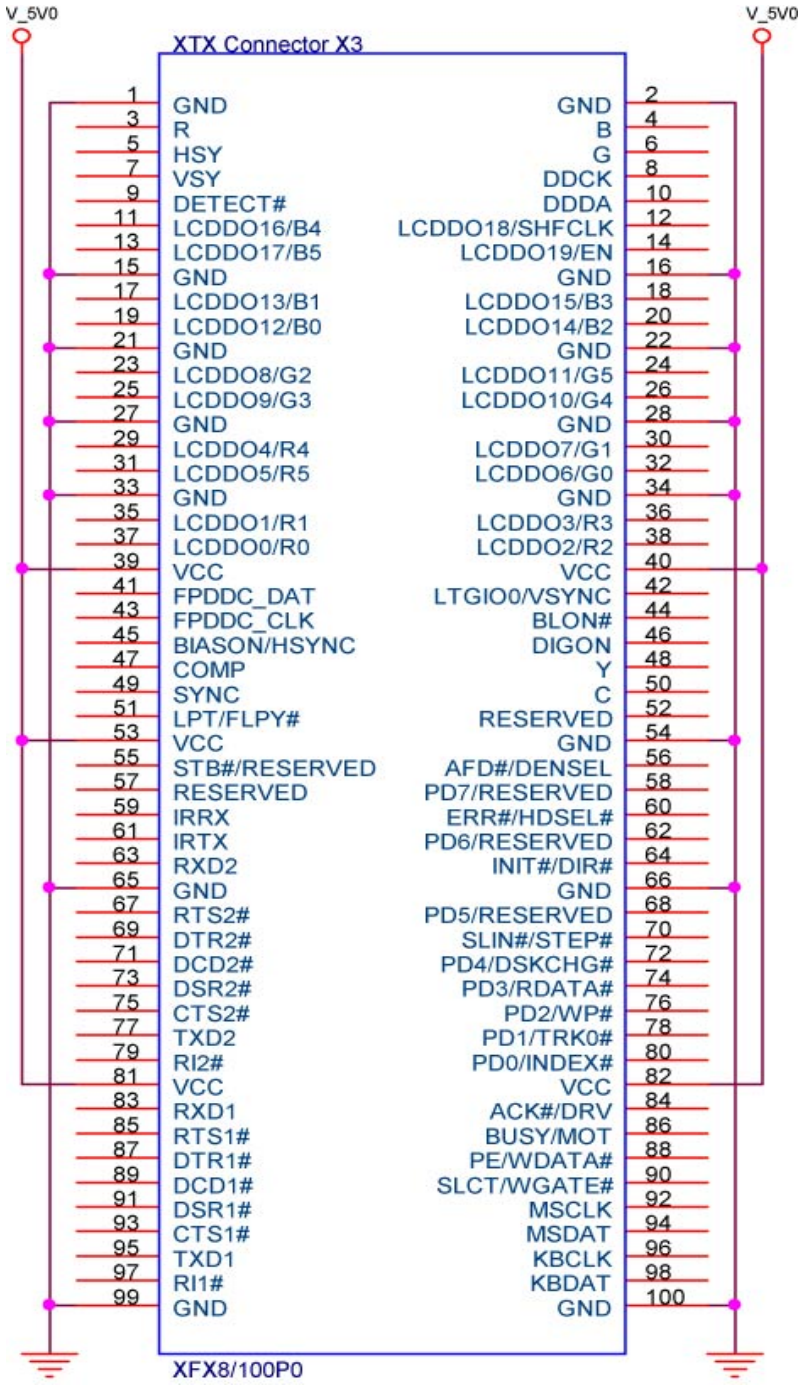
4.1 XTX™ Connector X1



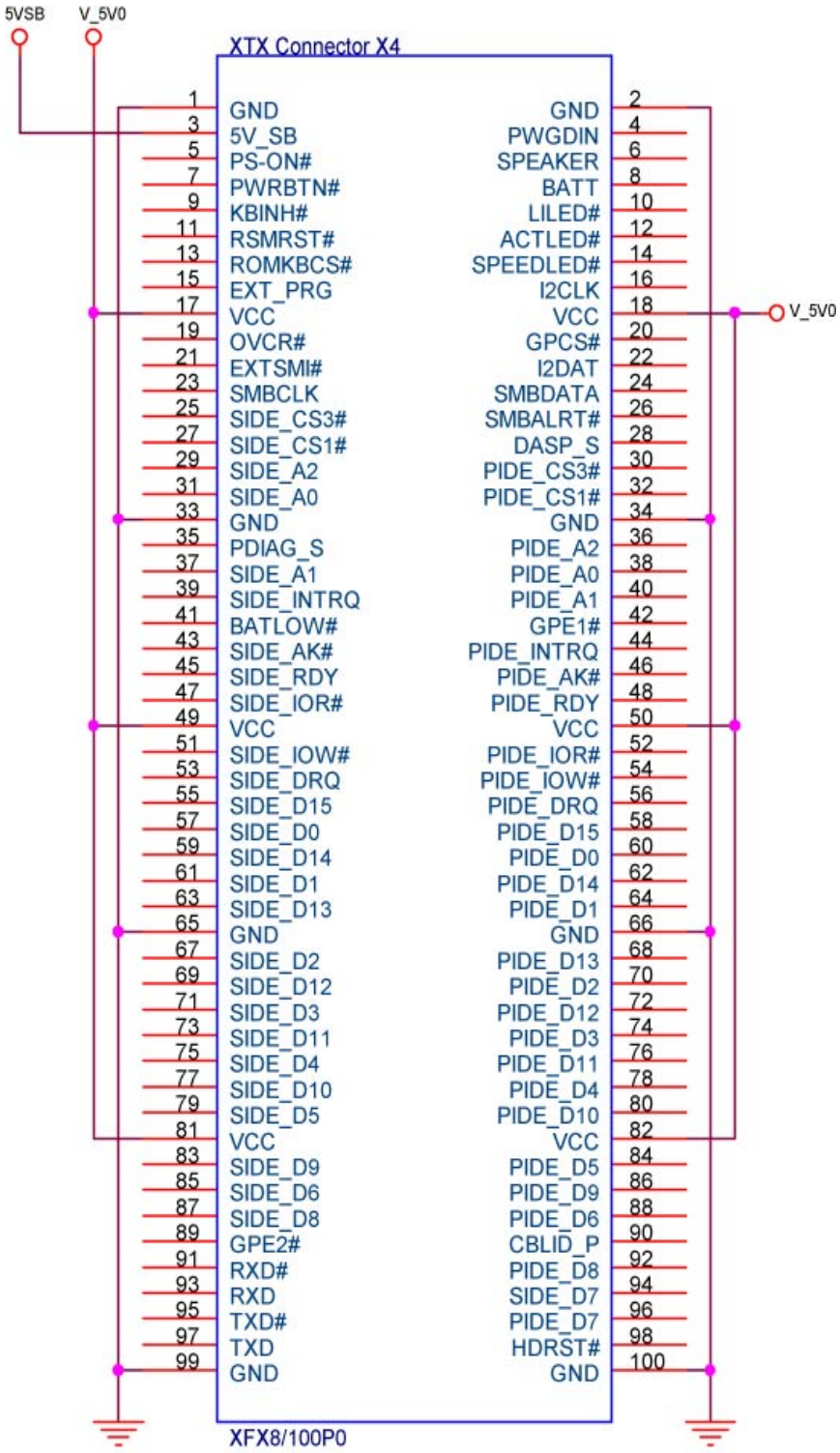
4.2 XTX™ Connector X2



4.3 XTX™ Connector X3



4.4 XTX™ Connector X4



5 XTX™ Implementation Specification

5.1 PCI Express

According to the PCI Express Base Specification Revision 1.1, a total available interconnect loss budget of 13.2 dB is allowed between the PCI Express device (chipset) on the XTX™ CPU module and the PCI Express device on the carrier board, Express Card or PCI Express add-in card.

The electrical characteristic at the XTX™ CPU module is defined in terms of electrical budgets. This budget allocation decouples the electrical specification for the carrier board designer and the XTX™ CPU module vendor. Unless otherwise noted, the specifications contained herein apply to all high-speed signals of each interface width definition. The signaling rate for encoded data is 2.5 G transfers/s and the signaling is point-to-point.

5.1.1 XTX™ Module Budget Allocation

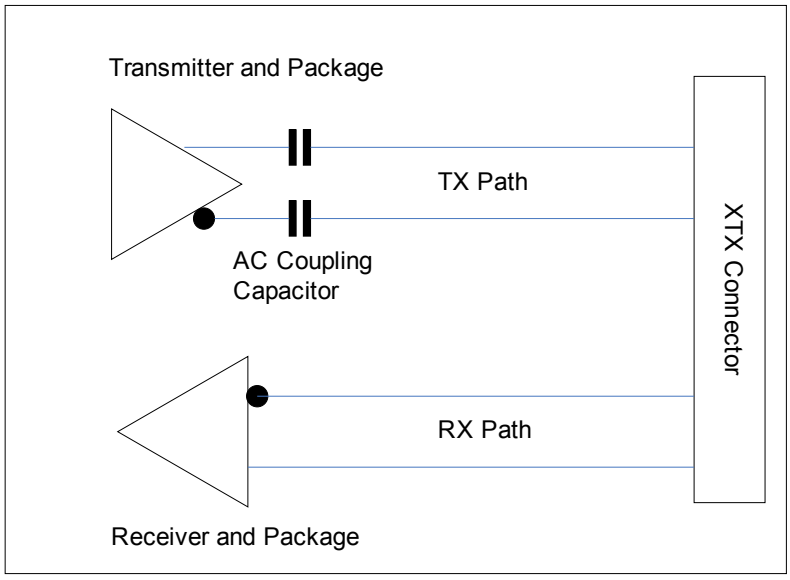


Figure 1 XTX™ PCI express Interconnect

Table 31 XTX™ Module Budget Allocation

Segment	Loss Budget Value at 1.25 GHz (dB)	max. Trace Length	Comments
XTX™ Module (TX path)	< 2.5	2 inches	Note 1, 2, 3, 4, 5, 6
XTX™ Module (RX path)	< 2.1	2 inches	Note 1, 2, 4, 5, 6

Notes

1. *The PCI Express Base Specification allows an interconnect loss of 13.2 dB for 1.25 GHz signals. The allocated XTX™ loss budget does not include crosstalk and impedance mismatch. As a guide for design and simulation, the PCI Express CEM Specification recommends to subtract 5.2 dB from the 13.2 dB budget, to cover crosstalk and impedance mismatch for the total interconnect path. The 5.2dB budget also includes the overall 1.25dB guardband as recommended by the PCI CEM specification*

2. *This budget also includes the mated connector on the carrier board. The budget allocated to the XTX™ connector is 1.0dB.*

3. *The TX path budget includes the additional damping of the DC decoupling capacitors*

4. *Typical damping of the PCB trace of 0.35dB/inch @ 1.25GHz (common value for FR-4 based material)*

5. *Maximum 2 vias per trace for a RX pair and maximum 4 vias per trace for a TX pair on the connection from the core logic chipset to the XTX™ connector on the XTX™ module.*

6. *Trace routing is implemented according to the design rules for high speed differential traces.*

5.1.2 Carrier Board Loss Budget Allocation

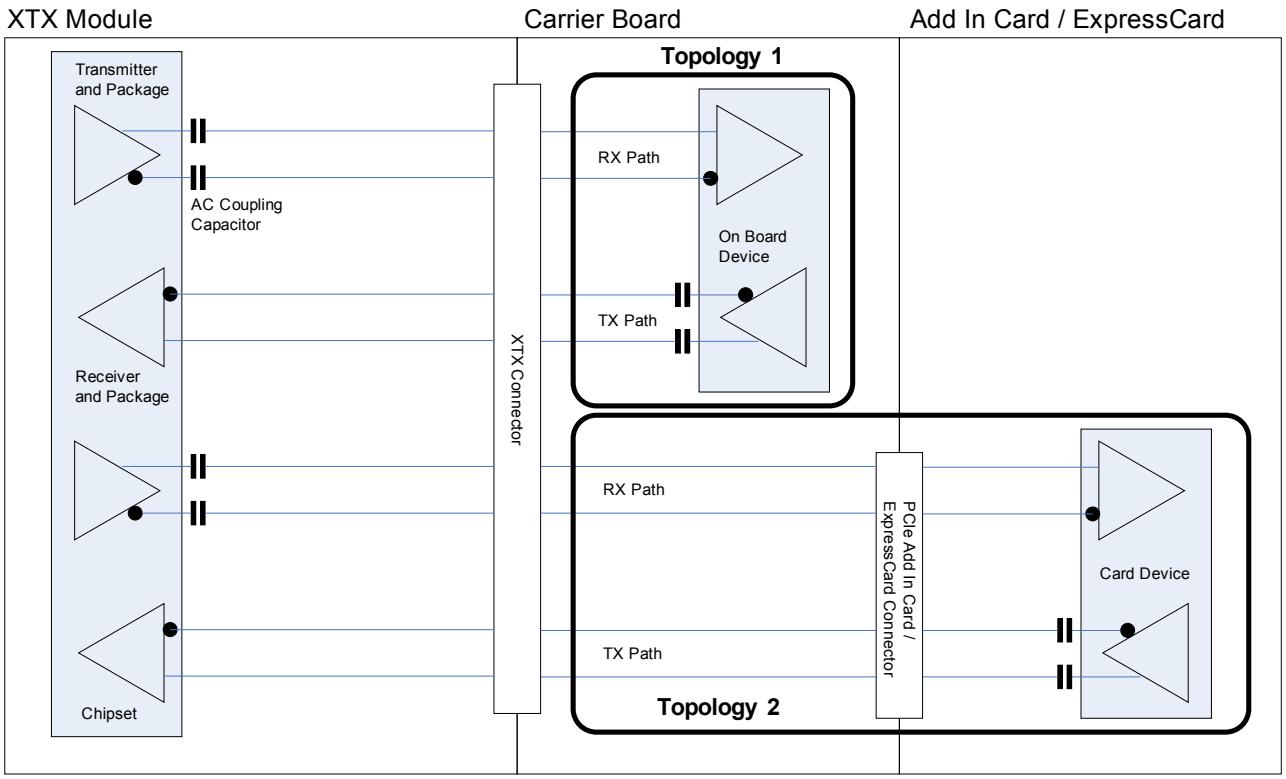


Figure 2 PCIe Topology

Note

The term "TX-path" that is used in the following refers to the signal path from the PCIe transmitter on the XTX™ module to the PCIe receiver, of an onboard device or on an add-in card, on the XTX™ carrier board.

The term "RX-path" that is used in the following table refers to the signal path from the PCIe transmitter, of an onboard device or on an add-in card on the XTX™ carrier board, to the PCIe receiver on the XTX™ module.

Table 32 Carrier Board Loss Budget Allocation

Segment	Loss Budget Value at 1.25 GHz (dB)	max. Trace Length	Comments
Carrier Board Topology 1 (TX path)	5.5dB	14.5 inches	Carrier Board with onboard PCI Express device
Carrier Board Topology 1 (RX path)	5.9dB	15.7 inches	Carrier Board with onboard PCI Express device
Carrier Board Topology 2 (TX path)	4.1dB	7.7 inches	Carrier Board with PCI Express Connector for Add-In Card or ExpressCard
Carrier Board Topology 2 (RX path)	4.1dB	7.7 inches	Carrier Board with PCI Express Connector for Add-In Card or ExpressCard

The trace length presented in table 10 are based on the following assumptions:

- Typical damping of the PCB trace of 0.35dB/inch @ 1,25GHz (common value for FR-4 based material)
- The RX path budget includes the additional damping of the DC decoupling capacitors and 2 additional vias for connecting the decoupling capacitors
- Maximum 2 vias per trace for a RX pair and maximum 4 vias per trace for a TX pair on the connection from the the XTX™ connector on the XTX™ carrier board to an onboard device
- Maximum 2 vias per trace for a RX pair and maximum 2 vias per trace for a TX pair on the connection from the the XTX™ connector on the XTX™ carrier board to a PCIe extension socket that is compliant to the properties defined in the PCIe CEM specification (this includes standard PCIe cards as well as ExpressCards).
- Trace routing is implemented according to the design rules for high speed differential traces.

The values in tables 9 and10 are derived from a signal integrity simulation and reflect a worst case scenario. The values given are design rules for a maximum interoperability between XTX™ modules from different vendors and customer specific XTX™ carrier boards and shall be followed in common. Designers that face the necessity to deviate from the given values have to conduct a suitable signal integrity simulation to guarantee compliance to the XTX™ specification and the underlying PCI Express specification. Carrier boards that do not follow the design rules presented in this specification and those that have not been simulated are not considered XTX™ compliant.

For carrier board designers that want to set up a simulation environment they should contact their XTX™ module vendor to obtain an XTX™ module model for signal integrity simulation.

Note

Design guidelines for high speed differential traces can be found in the XTX™ design guide.

5.1.3 Trace and Routing Parameters

In order to comply with the PCI Express CEM and Base specifications, the following trace and routing parameters need to be observed:

- Trace impedance: **100 Ohms +/- 20%** (including all variations due to production processes)
- Pair to pair skew on XTX™ module (only applies to modules that support x2, x4 link configurations): **0.5ns maximum**
- Pair to pair skew on XTX™ carrier board with PCIe add in card (topology 2) (only applies to modules that support x2, x4 link configurations): **0.75ns maximum**
- Pair to pair skew on XTX™ carrier board with PCIe onboard component (topology 1) (only applies to modules that support x2, x4 link configurations): **1.1ns maximum**
- Trace to trace skew within a differential pair on XTX™ module: **5mil maximum**
- Trace to trace skew within a differential pair on XTX™ Carrier Board with PCIe add-in card (topology 2): **5mil maximum**
- Trace to trace skew within a differential pair on XTX™ Carrier Board with PCIe onboard component (topology 1): **10mil maximum**

5.2 SATA Gen1

Based on the SATA Specification in addition with recommendations from different Chipset vendors use following budgets for the SATA implementation on the XTX™ module and carrier board.

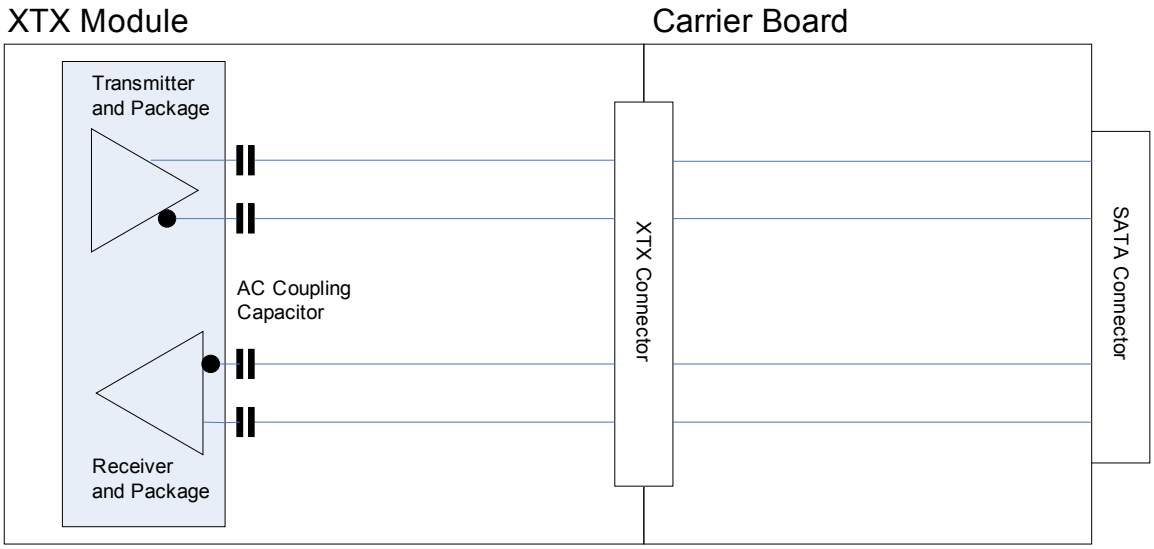


Figure 3 SATA Topology

Table 33 SATA Loss Budget Allocation

Segment	Loss Budget Value at 1.5 GHz (dB)	max. Trace Length	Comments
XTX™ Module	2.52 dB	2.5 inches	including Coupling Caps and mated XTX™ Connector
Carrier Board	1.68 dB	4 inches	

The trace lengths presented in table 11 are based on the following assumptions:

- Typical damping of the PCB trace of 0.42dB/inch @ 1,5GHz (common value for FR-4 based material)
- The Budget includes the additional damping of the DC decoupling and the XTX™ connector losses.
- Trace routing is implemented according to the design rules for high speed differential traces.

6 Industry Specifications

The list below provides links to industry specifications used to define the XTX™ interface specification.

Specification	Link
Audio Codec '97 Component Specification, Version 2.3 (AC '97)	http://www.intel.com/design/chipsets/audio/
Low Pin Count Interface Specification, Revision 1.0 (LPC)	http://developer.intel.com/design/chipsets/industry/lpc.htm
Universal Serial Bus (USB) Specification, Revision 2.0	http://www.usb.org/home
PCI Bus specification Revision 2.1 PCI Express Base Specification, Revision 1.1 PCI Express Card Electromechanical Specification, Revision 1.1	http://www.pcisig.com/specifications
Serial ATA Specification, Revision 1.0a	http://www.serialata.org
HIROSE Catalog "FX8 SERIES"	http://www.hirose-connectors.com